Performance analysis of high-speed, low-power comparators

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Abstract. This article mainly presents a summary of development of dynamic comparators and the optimization to conventional comparator in recent years. By comparing the design of two different comparators, the design method of less power consumption, high speed or small delay, and low input referred noise can be concluded. The Dynamic comparator is designed to have small delay and less power consumption compared with two-stage comparator. The dynamic-bias comparator spends less power for operation the circuit compared with double-tail comparator. The FIA comparator operates under the controlling of logic NOR gate.

Keywords: two-stage comparator, dynamic-bias comparator, FIA comparator

1. Introduction

The use of the comparator and its status is constantly improving with the development of technology. It is usually used in integrated biomedical systems and comparing the magnitude of the absolute value of two values. In generally, the working principle of the comparator is to input two analog inputs at the terminals of the comparator, and output a digital value, either 0 or 1, which is logic low or logic high, respectively. This is also known as ANALOG-TO-DIGITAL converters (ADCs).

The conventional dynamic comparator is called Strong-ARM comparator, which was the first class of dynamic comparator and used in many different area and field. There are some important features that Strong-ARM has, the positive feedback of the latch is strong enabling the fast decision; it does not consume static power; rail-to-rail output can be produced; input referred offset is small; and the input impedance, Zin, is high. Basically, the architecture of Strong-ARM is to stack pre-amplifier and latch as shown in the Figure 1 [1].

However, as the requirements continue to increase, the size of each MOS transistor need to be reduced, so that the more devices can be embedded into the IC. [1]. What does Figure 2 show is that stacking the transistors can be mitigated by cascading the transistor using double-tail latch type comparator.

However, this double-tail comparator also has problem, which is the higher power consumption.

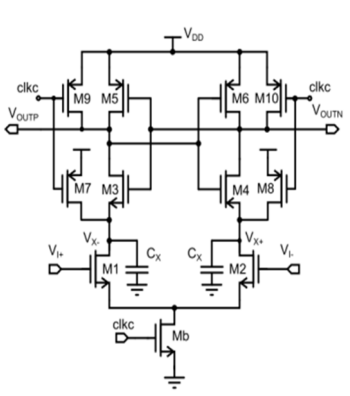


Fig 1. Strong-ARM comparator

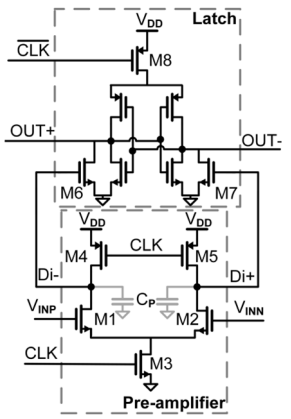


Fig.2. double-tail comparator

What does Figure 3 show is two-stage dynamic comparator. Each stage is charged by VDD. There are also serval advantages of two-stage comparator, which provide a more adjustable compromise between speed and offset and reduced kickback noise, it is more suitable when the VDD is relatively low compared with conventional comparator [2].

However, only PMOS device is operating before the phase that OUT_p and OUT_n are charged to the threshold voltage of NMOS since NMOS is off when it is not reached to the threshold voltage. Therefore, the energy consumption and delay are high. [3]. What is shown in the Figure 4 is the waveform of two-stage comparator. It is included the CLK, OUT_p, and OUT_n voltages we have discussed above. Furthermore, it is included an extremely important parameter in comparator design, delay. This can be divided into two parts, t_0 and t_{latch}. Positive edge of CLK voltage to both OUT_p and OUTn charged to the V_{tn} is the period that t_0 represents. What does t_{latch} represent is the period from the end of t_0 to the time when the V_i of the OUT_p and OUT_n reaches VDD/2, which can be observed when OUT_p =0.7V and OUT_n =0.1V, VDD is charged to 1.2V [3].

This paper is divided to five parts. The improvement design and comparative analysis of two-stage dynamic comparator will be introduced in Part II; that of double-tail comparator will be introduced in Part III; that of dynamic-bias will be introduced in Part IV. Part V will be the conclusion of this paper.

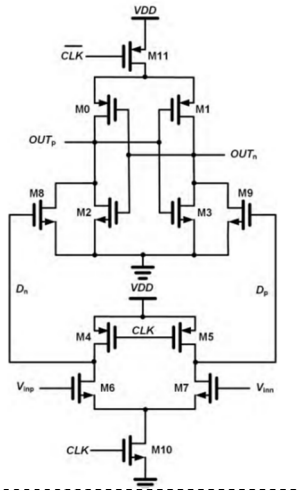


Fig.3. Two-stage comparator

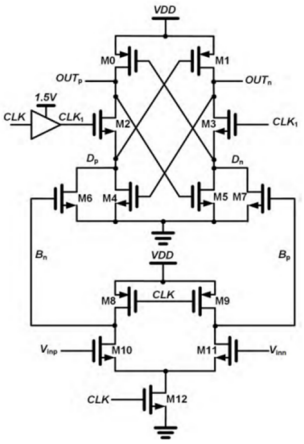


Fig.5. Improvement design of two-stage comparator

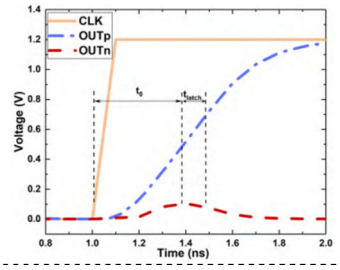


Fig.4. Waveform of Figure 3 design

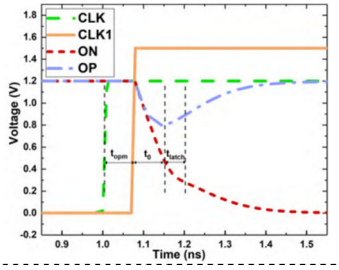


Fig.6. Waveform of the design shown in Figure 5

2. Switch Separated Comparator

As shown in the Figure 5, the improvement design of two-stages comparator is presented. The old latching stage is replaced by using serval cross-coupled pairs. The logic of this design is B_p and B_n will be charged to the VDD, M2, M3 will be turned off, M0, M1, M6 and M7 will be turned on when CLK is equal to zero. Node D_p and D_n will be discharged to ground passing through the M6 and M7.

Nodes OUT_p and OUT_n will be charged to VDD passing through the M0 and M1 [4]. This is a big changing relative to origin design.

As shown in the Figure 6, both OUP_p and OUT_n start with a relatively high voltages, which means NMOS is no longer to operate in the cut-off region during the period t_0. All of transistor can operate at the beginning, the comparison phase will be started faster. [3]. Moreover, t_{opm} is added into the chart. This parameter is the period from the positive edge of CLK to that of CLK1. [5].

Figure 7 shows the graph of $g_{m,eff}$ (total transconductance) of the traditional and improved comparators versus delay. Figure 8 shows that the graph of delay and power consumption versus width M2 and M3.

Transconductance of this device is larger, its delivering capability is greater. Therefore, having a large transconductance is necessary for the design. By observing Figure 7, it can be concluded that the total transconductance is the highest when the delay is roughly 230ps to 240ps. We are able to compare these two graphs to determine the best width of M2 and M3. By observing Figure 8, there is one option for the width which satisfies the range of delay, from 230ps to 240ps. Therefore, when widths of these two transistors are 0.75μm, $g_{m,eff}$ is the largest, so that the gain will be also the largest. And for the very significant factor, power consumption, when the widths are 0.75μm, the power consumption is relatively low, roughly 54.5μw.

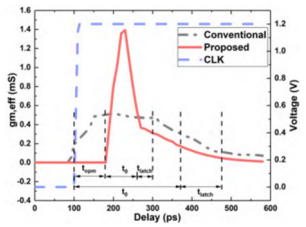


Fig.7. Simulated $g_{m,eff}$ of the traditional and improved comparators.

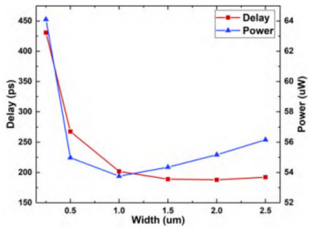


Fig.8. Delay and power versus width of the switch transistor.

By observing Figure 9 (a) and (c), it can be seen that when V_{cm} is between 0.8V and 1.2V, the delay and power consumption are relatively low, but our design ideas must also follow to make the whole circuit operate in a stable status, So V_{cm} ended up being between 0.9V to 1.1V is reasonable. Moreover, by observing the Figure 9 (e), the lines when V_{cm} not being between 0.9V to 1.1V can be ignored. As we can see, the lines which represent V_{cm} is 0.9V, 1.0V and 1.1V are close to each other, which means the delay is close to each other when V_{cm} is 0.9V to 1.1V, the circuit operate stable.

The way we choose for VDD is the same as we choose for V_{cm}. However, as shown in the Figure 9 (b) and (d), in the process of increasing VDD, its relationship with delay and power consumption is not the same as V_{cm} relationship with those. With the increasing of VDD, the delay is decreasing but the power consumption is increasing. Therefore, we cannot choose the best VDD to satisfy both delay and power consumption are low but make a compromise. Moreover, it is necessary to consider about the relationship between VDD and V_{cm}. They cannot be too close.

The whole circuit can be simulated when the V_{cm} is 0.9V to 1.1V and VDD is 1.0V to 1.2V. When we make the simulation, both increment of VDD and V_{cm} should be 0.02V in order to make 100 testcases. After the simulation, the best and reasonable VDD and V_{cm} for this circuit design can be got.

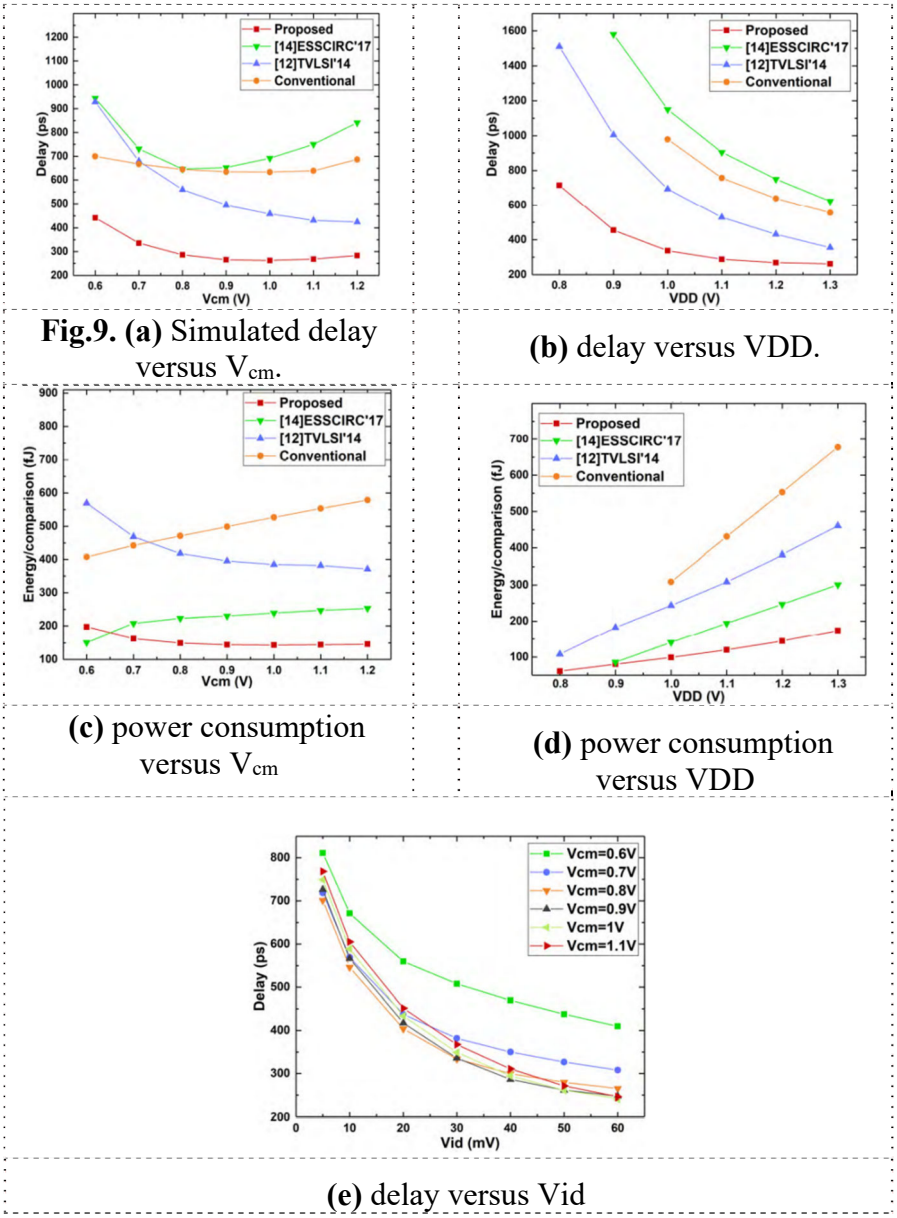


Fig.9. (a) Simulated delay versus V_{cm}.

(b) delay versus VDD.

(c) power consumption versus V_{cm}

(d) power consumption versus VDD

(e) delay versus Vid

3. Dynamic Bias Comparator

As shown in the Figure 10, this circuit is designed to improve the double-tail comparator by adding a capacitor and another CLK input that is parallel with the capacitor. Since the conventional double-tail circuit needs to be charged and discharged every time it is turned on and off, so its power consumption will be very large [6]. As we discussed above, the improvement is to stabilize the pre-amplifier by adding this capacitor, C_{TAIL}, at the end of tail of comparator. The reason of connecting transistor M3b parallel to C_{TAIL} is to reset this capacitor to ground. During the reset phase, when the logic of CLK is equal to 0, so, D_{i+} and D_{i-} are pre-charged to VDD by connecting M4 and M5. The capacitor C_{TAIL} is used to discharge to the ground. M12 and M13 are used to reset the latch. M3b, M4, M5, M12, and M13 are reset transistors. During the comparison phase, when the logic of CLK is equal to 1, which is VDD, these reset transistor are turned off [7]. CLK input, which is M3a, and capacitor, CP, are both turned on so that the discharge of the drain nodes Di+ and Di- begins.

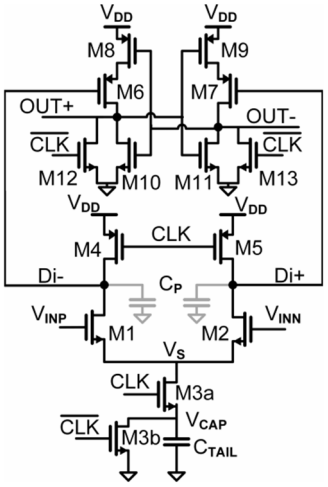


Fig.10. Improvement circuit of double-tail comparator, dynamic-bias.

The Figure 11 shows the voltage of different parameters versus time. As we can see at Figure 11 (a), the voltage of drain node D_{i+} and D_{i-} start to decrease when t is roughly equal to 0.3ns, and it will ultimately drop to Vs. Thus, it should be recharge to 1.2V, which is VDD next time, which will cause a big power consumption. So we can see the same parameters in Figure 11 (b), their voltages are no longer dropped to Vs. So next time during the charging phase, the voltage needed to be charged to VDD will be small enough. Compared with the Figure 12 (a), it is clearer that the dynamic-bias design will not drop to zero volt with the time elapse, but the Elzakker will drop to zero volt. From Figure 12 (c), it indicates the current passing through the tail, for the dynamic-bias, the current will decrease to zero immediately after the comparing phase, but for the Elzakker, the current slowly decreases to zero. According to the formula of power with respect of voltage and current, the larger power consumption will be produced for Elzakker [4].

However, the problem of this dynamic-bias design is shown in the two bottom figures, which the delay of the circuit increases as power consumption decreases. For the Elzakker, the interval between the start of CLK and OUT_+ is roughly 0.45ns, but for the dynamic-bias, the interval of that is roughly 0.7ns. This problem can be also observed in the Figure 12 (b).

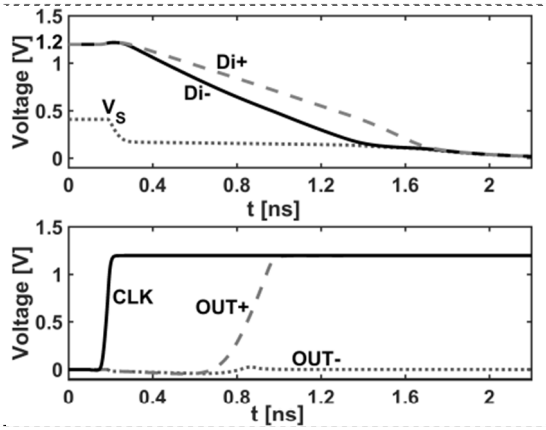
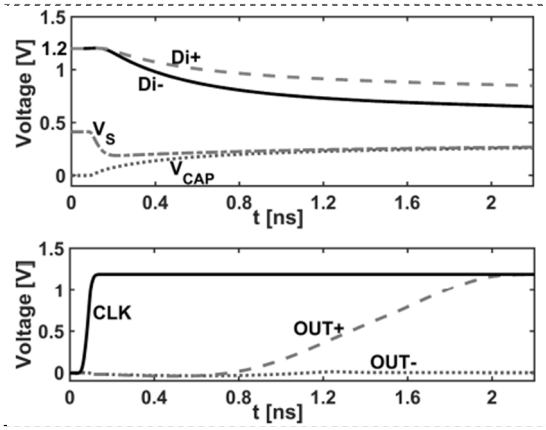


Fig.11. (a) simulated timing waveform of conventional double-tail comparator for 'Elzakker'.



(b) timing waveform of dynamic-bias, $|V_{in}|$ = 0.025V at V_{cm} =0.6 V and VDD = 1.2 V.

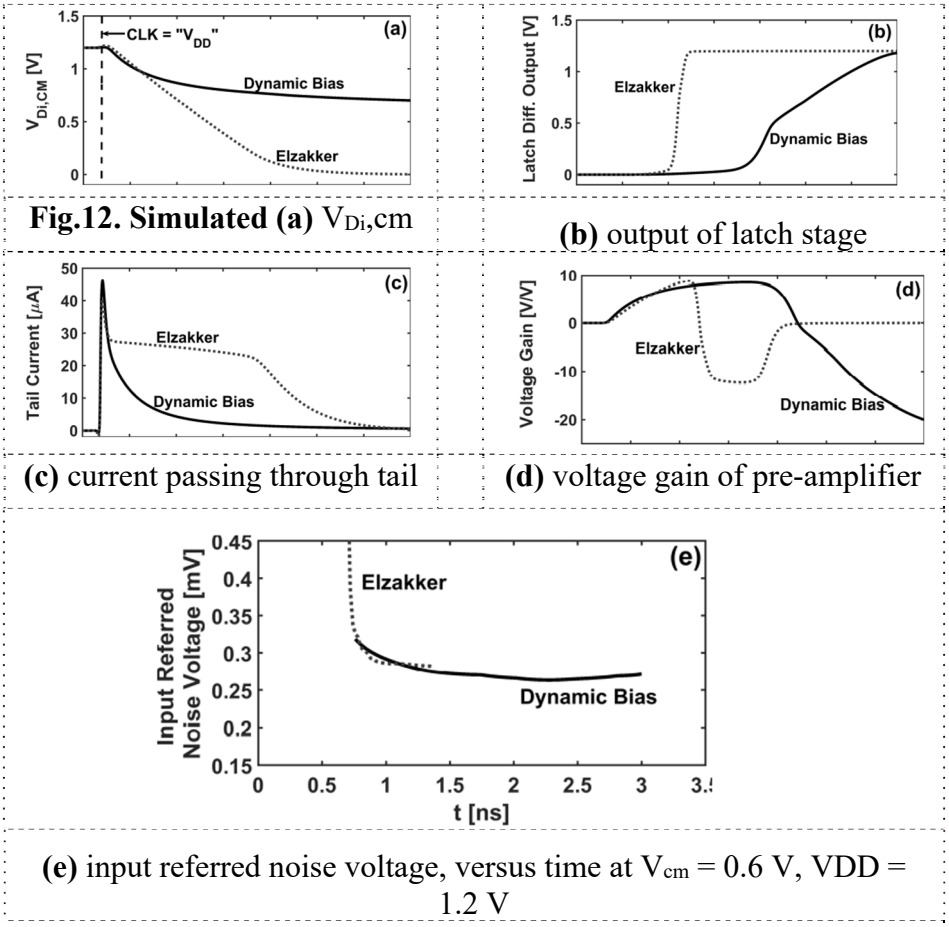


Fig.12. Simulated (a) $V_{Di,cm}$ **(b)** output of latch stage **(c)** current passing through tail **(d)** voltage gain of pre-amplifier **(e)** input referred noise voltage, versus time at V_{cm} = 0.6 V, VDD = 1.2 V

The improvements of this dynamic-bias are not only lower power consumption, but also higher voltage gain, and lower input referred noise. As shown in the Figure 12 (d) and (e), voltage gain of dynamic-bias stays in very high, the input referred noise voltage of dynamic-bias stays in very low, compared to Elzakker.

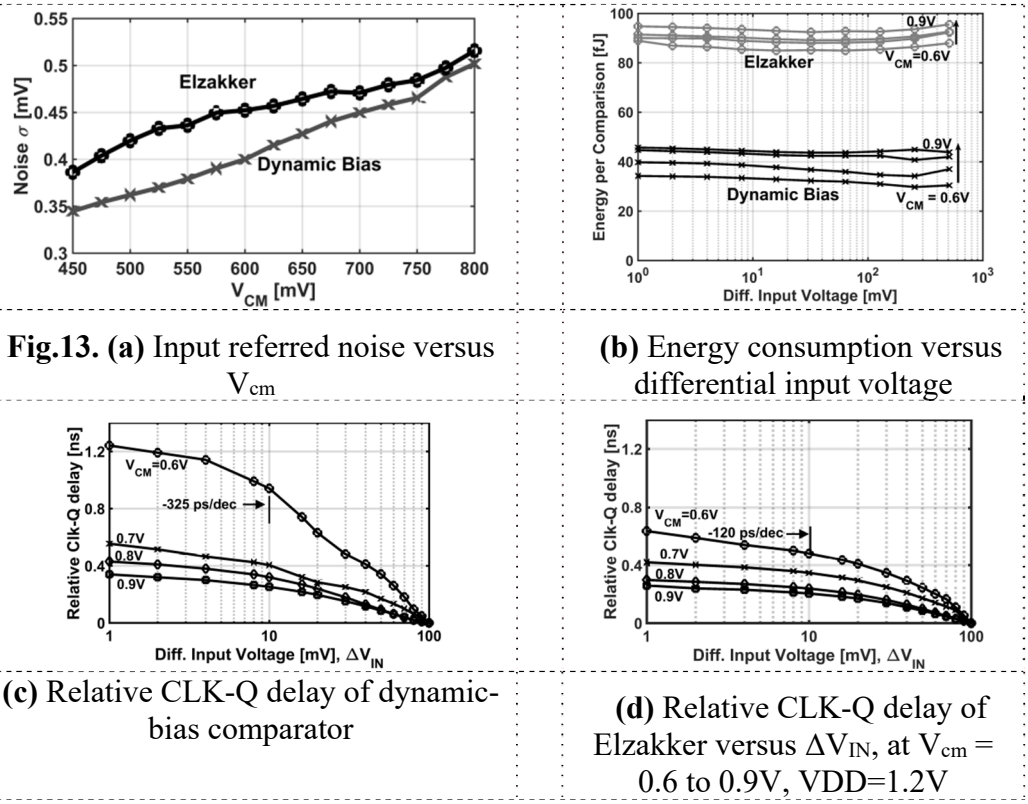


Fig.13. (a) Input referred noise versus V_{cm} **(b)** Energy consumption versus differential input voltage **(c)** Relative CLK-Q delay of dynamic-bias comparator **(d)** Relative CLK-Q delay of Elzakker versus ΔV_{IN}, at V_{cm} = 0.6 to 0.9V, VDD=1.2V

From the Figure 12 (b), Dynamic-bias consistently consumes less energy than Elzakker no matter at what the common mode voltage, and that of dynamic-bias is very stable at V_{cm} = 0.6V to 0.9V, which is a good improvement. By observing the (c) and (d), the delay of dynamic-bias is much larger than that of Elzakker when the V_{cm} = 0.6V, but if we increase the V_{cm} to 0.7V, the delay will be significantly reduced and very close to the delay of Elzakker at V_{cm} = 0.7V. However, by observing (a), it is easy to find out that the input referred noise will increase when the V_{cm} increases, which prevents us from arbitrarily increasing V_{cm} to meet the standard of lower delay. Therefore, we can make a trade-off between delay and input referred noise. The V_{cm} can be chosen from 0.6V to 0.75V with an added noise cost of 0.16mV. Thus, we can simulate and test the result of delay when V_{cm} is from 0.6V to 0.75V, the increasement of simulation is 0.0015V for getting 100 test cases [8].

4. Floating Inverter Comparator

As we discussed above, although the power consumption and input referred noise of dynamic-bias are much lower than the conventional double-tail design, its delay is much larger than the conventional design when the V_{cm} is 0.6V, and the VDD is 1.2V. The Figure 14 shows the circuit that is designed based on the dynamic-bias but make a improvement on delay.

The logic of circuit shown in the Figure 14 is similar to dynamic-bias. In the pre- amplifier statge, C_{RES} connected to VDD and GND are charged under the three-terminal NOR gate of CLK, D_{o-}, and D_{o+}. When the pre-amplifier needs to operate, the NOR gate is disconnected [9]. At this time, C_{RES} and the pre-amplifier are connected in parallel so that the pre-amplifier is not connected to the power supply and is charged by C_{RES}. Also there will be no static current passing through. In the latch stage, there is a transistor CLK connected to PMOS to stablize [10].

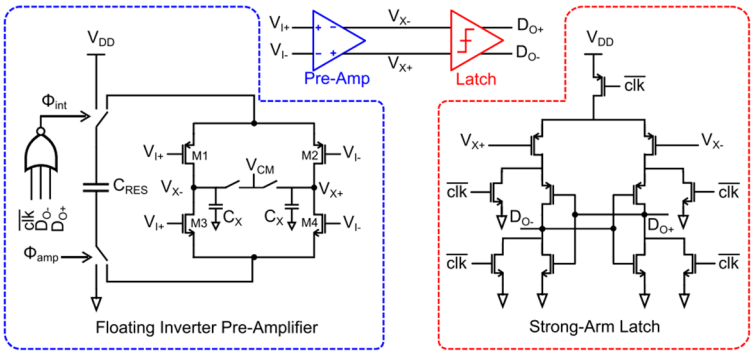


Fig.14. The improement design of dynamic-bias

As shown in the Figure 15, with the increasing of input V_{cm} of pre-amplifier, output common-mode voltage and gain are decreasing. By observing (b), the delay is larger than Strong-ARM when the input V_{cm} is from 0.6V to 0.8V, and the output V_{cm} and gain also have significant decline when Vi,cm is from 0.6V to 0.8V. Moreover, by observing (c), the input referred noise does not have a obvious fluctuation when Vi,cm is from 0.5V to 0.8V. Therefore, the reasonable range of input V_{cm} is from 0.45V to 0.55V.

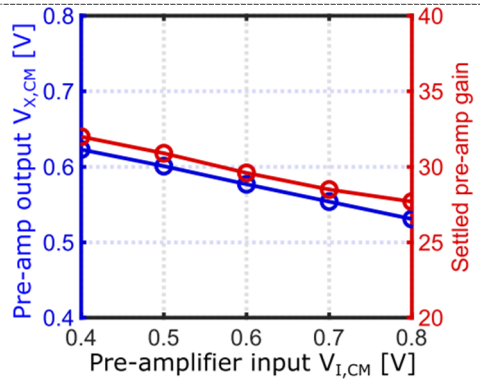
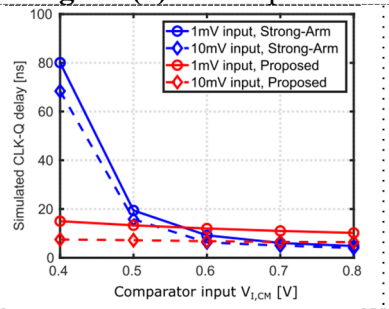
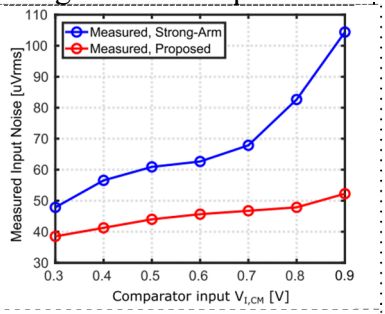


Fig.15. (a) Pre-amplifier Vx,cm and gain versus input V_{cm}



(b) CLK-Q delay versus Vi,cm.



(c) Input referred noise versus Vi,cm.

What does show in the Figure 16 is the relationship between delay and power consumption, it can be interpreted from the unit of FoM, and the value of C_{RES}. By following the small delay and low power consumption, the value of C_{RES} that goes from 2 pF to 3.5pF is reasonable. Therefore, we can make a simulation with increasement of 0.01pF to see the delay and power consumption are both smaller and lower in which the value of C_{RES} is rational. From the observation, it is rational when C_{RES} is 3pF.

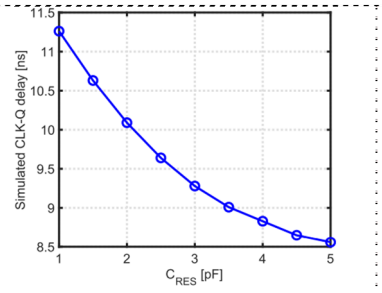
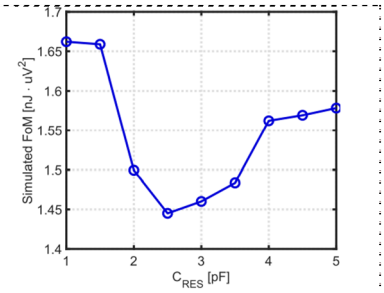


Fig.16. (a) CLK-Q delay



(b) FoM of the improved comparator versus the value of C_{RES}.

The variation of input offset of proposed comparator is 0.9mV, shown in the Figure 17, which is much smaller than that of Strong-ARM. This means that the proposed comparator operates more stable.

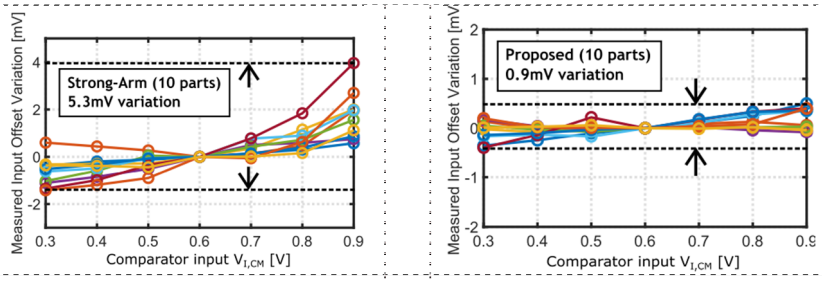


Fig.17. Measured 10 parts input offset of (a) StrongARM latch **(b)** improved comparator versus Vi,cm.

5. Conclusion

This paper concentrates on the optimization and reform method of comparator with consideration of three parameters, time delay, input referred noise, and power consumption. The first design optimizes the delay and reduce the power consumption of two-stage comparator by using the cross-couple method in latch stage. The second design is designed to solve the problem of power consumption of double-tail comparator by adding a CLK transistor and a capacitor, two parallel components, at the end of the tail, but delay is increased. This issue is solved in the third design by adding a CLK transistor connected to VDD in the latch stage and a capacitor controlled by a logic NOR gate with three different inputs. However, in the first reference paper, one of the most important parameters, input referred noise, is not mentioned and researched. Therefore, it is difficult to make the trade-off. Moreover, in the third reference paper, the comparator is designed based on the dynamic-bias comparator, but all of the simulations and measurements are compared to StrongARM comparator. Thus, it is difficult to directly observe the improvement of this design. It is necessary to simulate two comparators in the same condition. That is the what is going to do in the future researches.

References

[1] Tang X. 2020 An Energy-Efficient Comparator With Dynamic Floating Inverter Amplifier IEEE J. Solid-State Circuits. 55 1011-22.

[2] Bindra H. S., Lokin C. E., Schinkel D., Annema A.-J. and Nauta B. 2018 A 1.2-V dynamic bias latch-type comparator in 65-nm CMOS with 0.4-mV input noise IEEE J. Solid-State Circuits 53 1902–12.

[3] Wang Y., Yao M., Guo B., Wu Z., Fan W. and Liou J. J. 2019 A Low-Power High-Speed Dynamic Comparator With a Transconductance-Enhanced Latching Stage IEEE Access 7 93396-93403.

[4] Van Elzakker M., Van Tuijl E., Geraedts P., Schinkel D., Klumperink E. A. M., and Nauta B. 2010 A 10-bit charge-redistribution ADC consuming 1.9 μW at 1 MS/s IEEE J. Solid-State Circuits 45 1007–15.

[5] Liu M., Pelzers K., Van Dommele R., Van Roermund A. and Harpe P. 2016 A 106 nW 10 b 80 kS/s SAR ADC with duty-cycled reference generation in 65 nm CMOS IEEE J. Solid-State Circuits 51 2435–45.

[6] Akter M. S., Makinwa K. and Bult K. 2017 A capacitively-degenerated 100dB linear 20-150MS/s dynamic amplifier Proc. Symp. VLSI Circuits, Kyoto, Japan pp C136–C137.

[7] Ginsburg B. P. and Chandrakasan A. P. 2005 An energy-efficient charge recycling approach for a SAR converter with capacitive DAC Proc. IEEE Int. Symp. Circuits Syst 1 184–7.

[8] Tang X., Chen L., Song J. and Sun N. 2017 A 1.5 fJ/conv-step 10b 100 kS/s SAR ADC with gain-boosted dynamic comparator Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC) pp 229–32.

[9] Sepke T., Holloway P., Sodini C. G. and Lee H.-S. 2009 Noise analysis for comparator-based circuits IEEE Trans. Circuits Syst. I, Reg. Papers 56 541–53.

[10] Huang K., Luo D., Wang Z., Zheng X., Li F., Zhang C. and Wang Z. 2015 A 190 mW 40 Gbps SerDes transmitter and receiver chipset in 65 nm CMOS technology Proc. IEEE Custom Integr. Circuits Conf. (CICC) pp 1–4.