Analysis of the Improved Conventional Dynamic Comparator and the Edge-Pursuit Comparator

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Abstract: In order to understand and learn the comparator in detail, three kinds of comparator are analyzed in this paper. An improvement of the traditional dynamic double-tailed comparator. So as to get fast operation and low power in low supply voltages, the circuit of the traditional double-tailed comparator is modulated. Another one is an improved low-power comparator. During evaluation, we can activate its latch delayed in order to avoid excess power consumption and get sufficient preamplification gain. The most innovative design is named edge-pursuit comparator (EPC) which is a new energy-efficient ring oscillator collapse-based comparator. With changing the comparison energy on the basis of input difference uncontrolled, it can automatically adjust its performance. It can also eliminate unnecessary energy which is spent on coarse comparisons. In addition, we get analysis of the design which is in the phase domain in detail. It presents that the energy efficiency can be improved over traditional comparators even out of energy scaling.

Keywords: Comparators, Double-trail comparator, Edge-pursuit comparator, Phase domain.

1. Introduction

Nowadays, comparators are more and more important in many applications such as Current detection and digital to analog converter [1-3]. In some uses, the comparator's performance plays a significant role in the entire circuit, such as SAR, pipeline, and flash ADCs [4-6]. Considering the importance of comparators, many new designs of comparators have been proposed in recent years. Different designs have different concepts and can achieve different functions. Studying these designs will be of great help to our work.

Firstly, a modified dynamic comparator is proposed. By increasing $DV_{fn/fp}$ which can improve the regeneration speed of the latch, the circuit of the traditional double-tailed comparator [7] is adjusted to get a low-power and fast operation. Without complicating the design, the positive feedback can be strengthened in the regeneration phase, which results in remarkable reduction of delay.

Secondly, an improved low-power comparator is proposed and we can activate its latch delayed to avoid excess power consumption and reach sufficient preamplification gain at the evaluation phase. Furthermore, the proposed comparator can not only eliminate the problem inherently, but also make it possible to have the optimum delay efficiently. In this way, the power consumption is reduced and the speed is improved.

Finally, a new type of comparator named EPC is proposed. With changing the comparison energy on the basis of its input difference without any control, it can automatically adjust its performance. It can also eliminate unnecessary energy which is spent on coarse comparisons. Therefore, the designed topography can reach a great amount of energy saving about 86%. But the design doesn't take the delay into consideration. Due to the lack of analyzing of delay, the optimization of the delay time should be regarded in the future work as an important parameter in the analysis of the EPC.

2. Analysis of the devised comparator

2.1 Analysis of the improved Low-Power and Low-Voltage Double Tailed Comparator

In this section, the analysis about the delay of the comparators is shown and the analytical formulas will be obtained.

According to these formulas, we are able to explore the tradeoffs in the proposed design and get a sense of the decisive contributors to the delay.

For the sake of visualizing the performance of the design, the first thing we need to do is introducing the two conventional comparators, namely, the conventional double-tailed dynamic comparator and the conventional dynamic comparator (CDC) [8].

CDC's delay can be derived as follow:

$$\begin{aligned} t_{delay} &= t_0 + t_{latch} \\ &= 2\frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right) \end{aligned} \tag{1}$$

Due to several stacked transistors, the disadvantage of the CDC is the fact that if you wang to get a proper delay, you should firstly set an enough high supply voltage. Another important shortcoming is that it has merely one path of the current. In addition, since M_{tail} mainly operates in the triode region, the tail current which lies on the input common-mode voltage that isn't conducive to regeneration.

As for the traditional double-tailed dynamic comparator, the total delay is:

$$\begin{aligned} t_{delay} &= t_0 + t_{latch} = 2\frac{V_{Thn}C_{Lout}}{I_{tail}} + \frac{C_{Lout}}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \\ &= 2\frac{V_{Thn}C_{Lout}}{I_{tail}} + \frac{C_{Lout}}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}I^2_{tail}C_{L,f_n(P)}}{8V^2_{Thn}C_{Lout}g_{mR_{1,2}}g_{m1,2}\Delta V_{in}}\right) \end{aligned} \tag{2}$$

In the proposed comparator, the two middle stage transistors will eventually be aborted (because both f_n and f_p nodes discharge to GND), so they will have nothing to do to improve the effective transconductance of the latch. What's more, they need to be charged from the GND to the V_{DD} during resetting. In this way, it costs power consumption.

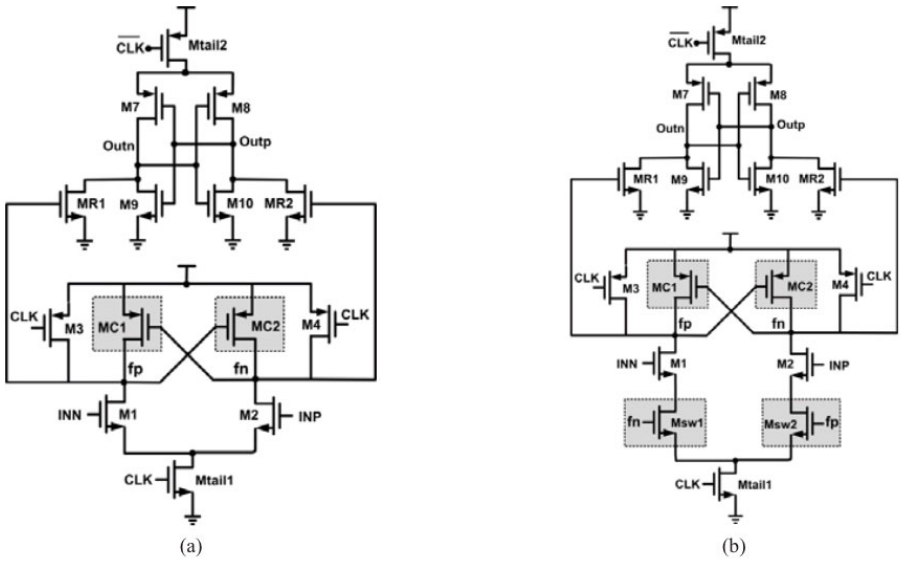


Figure 1. The raised dynamic comparator

We can see in the Figure 1, the schematic of the raised design which is designed on basis of the double-tailed structure on account of its better performance at low-voltage.

The operation of the raised design is shown below (Figure 2).

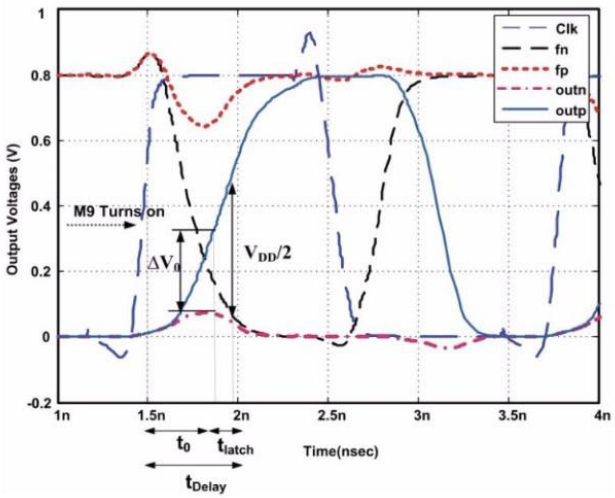


Figure 2. Operation of the proposed desgin

In the initial stage of the decision-making section, since both f_n and f_p nodes have been charged in advanced to the V_{DD} and all the on-offs are off, f_n and f_p begin to fall at different discharging speeds. If one of these nodes that the comparator detects is discharging faster, transistors which take the function of controlling will somehow augment their voltage difference. Assuming the f_p is pulled up to V_{DD}, the f_n must discharge fully. So, the on-off on f_p charging path will be turned on (to inhibit all of the current from being drawn out of the V_{DD}). However, the other on-off which is connected to the f_n is going to be turned off to permit the f_n node for discharging completely.

With affecting two significant factors, the raised comparator increases the double tailed comparator's velocity. The first one is increasing the original output voltage difference (V_0) ($t=t_0$) at the start of regeneration; The second one is improving the latch's effective transconductance (g_{meff}).

1) Effect about advancing DV_0:

$$\begin{aligned}\Delta V_0 &= 2V_{Thn}\frac{g_{mR_{1,2}}}{I_{tail2}}\Delta V_{f_n/f_p} \\ &= 4V_{Thn}\left|V_{Thp}\right|\frac{g_{mR_{1,2}}}{I_{tail2}}\frac{g_{m1,2}\Delta V_{in}}{I_{tail1}}\exp\left(\frac{G_{m,eff1}\cdot t_0}{C_{L,f_n(p)}}\right)\end{aligned} \tag{3}$$

2) Effect of Augmenting Latch Effective Transconductance:

$$\begin{aligned}t_{latch} &= \frac{C_{Lout}}{g_{m,eff}+g_{mR_{1,2}}}\cdot\ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) \\ &= \frac{C_{Lout}}{g_{m,eff}+g_{mR_{1,2}}}\cdot\ln\left(\frac{V_{DD}/2}{\Delta V_0}\right)\end{aligned} \tag{4}$$

Taking these into consideration, the total delay is:

$$\begin{aligned}t_{delay} &= t_0 + t_{latch} \\ &= 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}+g_{mR_{1,2}}}\cdot\ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \\ &= 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}+g_{mR_{1,2}}}\cdot\ln\left(\frac{V_{DD}/2}{4V_{Thn}\left|V_{Thp}\right|\frac{g_{mR_{1,2}}}{I_{tail2}}\frac{g_{m1,2}\Delta V_{in}}{I_{tail1}}\exp\left(\frac{G_{m,eff1}\cdot t_0}{C_L f_n(p)}\right)}\right)\end{aligned} \tag{5}$$

With comparing delay expressions of three structures, we can see that the proposed comparator makes use of internal positive feedback in the double tailed operation to augment the total function

that allows the latch to regenerate. The rate increase will be pronounced at lower supply voltages. It is on the basis of the fact that the transconductance of the transistor decreases with a larger V_{Th}/V_{DD} value. So, the presence of the internal positive feedback in the first stage structure will result in an improvement in the comparator performance. Simulation results prove this point.

The influence of the mismatch between the threshold and the current factor of the transistor which has the function of manipulating the complete input-referred offset voltage:

(1) Mismatch's effect which belongs to the threshold voltage:

$$\Delta V_{eq,due\Delta V_{Thc1,2}} = \frac{g_{mc1,2}\Delta V_{Thc1,2}}{g_{m1,2}} = \frac{\mu_p W_{C1,2} V_{ODC1,2}}{\mu_n W_{1,2} V_{OD1,2}} \Delta V_{Thc1,2} \tag{6}$$

(2) Current-Factor Mismatch's effect:

$$\Delta V_{eq,due\Delta\beta_{C1,2}} = \frac{i_{diff}}{g_{m1,2}} = \frac{0.5\mu_p W_{C1,2}(V_{gsc1,2} - V_{thp})^2}{\mu_n W_{1,2}(V_{gs1,2} - V_{thn})} = \frac{0.5\mu_p W_{C1,2} {V_{OD_{C1,2}}}^2}{\mu_n W_{1,2}(V_{cm} - R_{CLK} K_{nC1,2} {V^2}_{OD_{C1,2}} - V_{thn})} \tag{7}$$

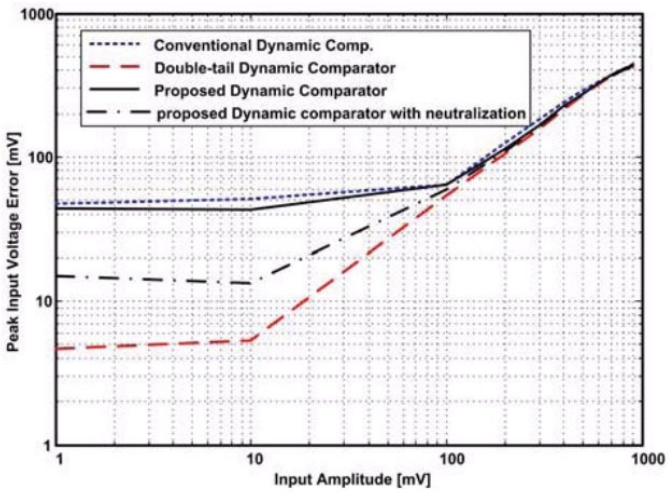


Figure 3. Crest input voltage mistake owing to kickback noise

Big voltage variations at regenerative nodes are coupled to the comparator input through the parasitic capacitance of the transistor. This often occurs in the latched comparators. Since the output hinder of the past circuit is bigger than zero, the input voltage is interfered that probably reduce the precision of the converter. Such interference is often referred to as "kickback noise" [9].

Although the proposed design advances the double-tail structure on the basis of operating velocity and energy that one comparison phase costs, the kickback noise is advanced compared to the traditional double-tailed design. Figure 3 illustrates the culminate perturbation as an operation of the differential input voltage in the mentioned structures. The proposed design takes use of the input-output isolation to minimize the kickback noise, while its kickback noise is resembled to the conventional one.

In the proposed comparator, however, due to the control of the transistors should not be as powerful as the latch transistors in CDC, it can size these transistors to maintain the advantages of increase of the speed and reduction of the power while reducing kickback noise. In addition, if

kickback becomes important in some applications, simple kickback reduction techniques can be applied, such as neutralization (Figure 3 presents the dynamic comparator with neutralization).

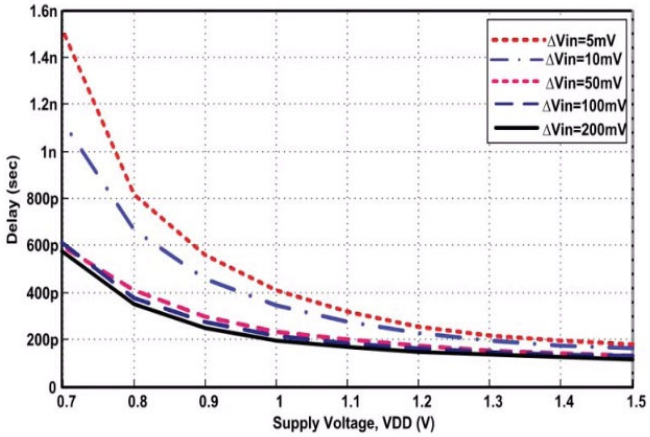


Figure 4. Delay versus V_{DD}

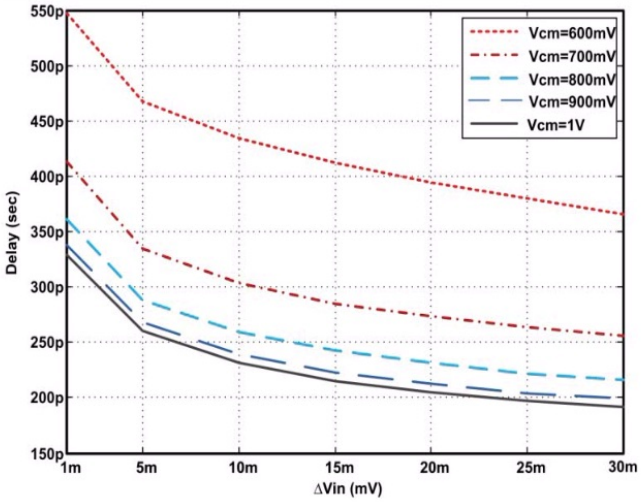


Figure 5. Delay versus DV_{in}

The energy and delay that one conversion costs of the raised design which are shown in the simulation results are greatly decreased compared with CDC and double-tail comparator.

2.2 Analysis of an improved Low-Power Comparator

This section describes a low-power comparator. The pMOS transistor is used for the input of the comparator's preamplifier likewise the latch stage. One special local clock generator controls both phases. During evaluating, the latch will be activated delayed to avoid excess power consumption and achieve sufficient preamplification gain. At the same time, for the sake of strongly switching on the pMOS transistor which is at the latch input and decreasing the delay, small cross-coupled transistor decreases the latch's input common mode and increases the preamplifier gain. The proposed design allows us to set optimal delay which is quite different from the conventional comparators.

So as to visualize the proposed design's performance, the first thing need to do is introducing conventional comparators.

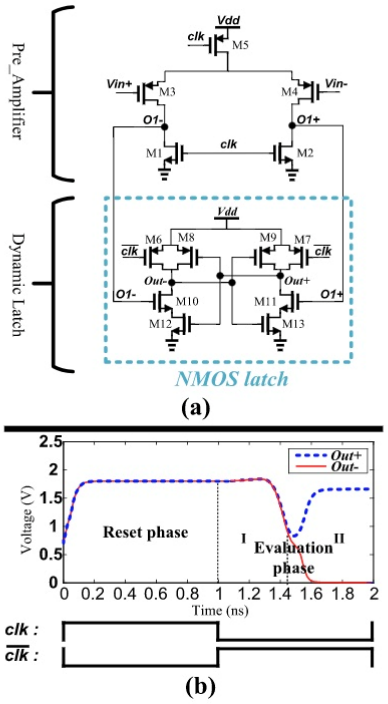


Figure 6. (a) Traditional two-stage comparator
(b) The classic output wavefrom and CLK

High power consumption is required to this low offset comparator. Furthermore, the speed of the latch limits its speed. What's more, it takes longer to charge the output voltage of the preamplifier stage to the rank above the nMOS threshold voltage. Also, once latch begins working, the rate is low because the delay should be long enough so that the latch can be triggered.

The proposed comparator can remove these problems and effectively makes it possible for a two-stage dynamic comparator [10] to have optimal delay. Thus, the power dissipation is reduced and the rate is increased.

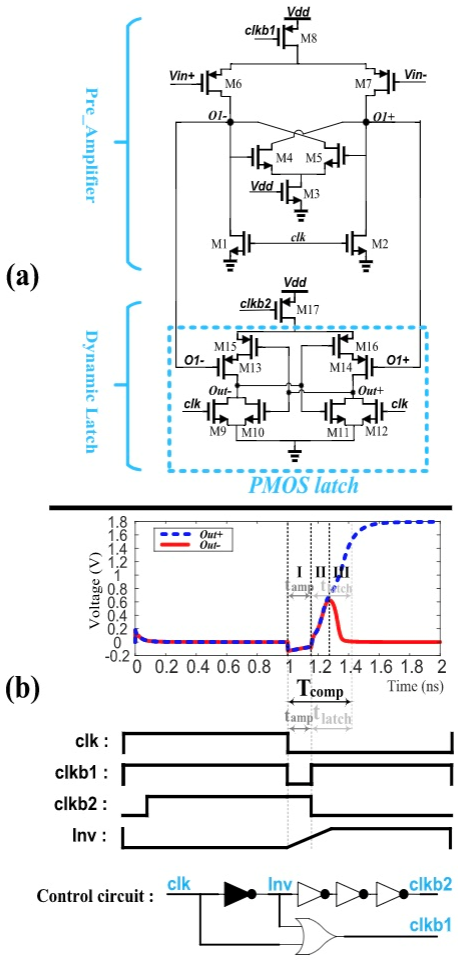


Figure 7. (a) Devised two-stage dynamic comparator (b) The classic output and CLK

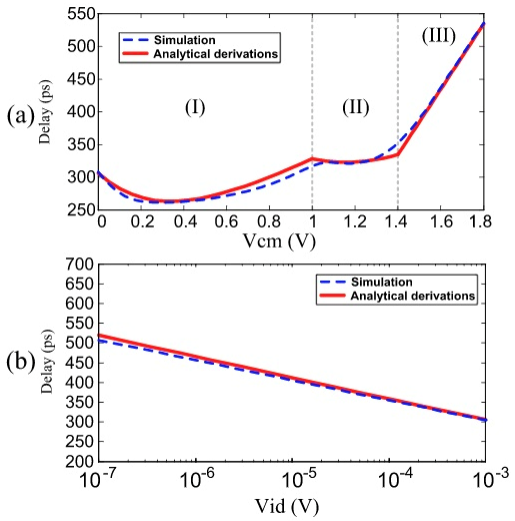


Figure 8. (a) Delay versus V_{cm} (b) Delay versus V_{id}

T_{comp}, the comparison delay of the design, is the sum of two parts. Firstly, the t_{amp} is presented in Figure 7(b), determined by the designer. And then, t_{latch} is that the latch requires to get sufficient swing at the output, depending on the input signal and the transistor latch stage's size.

t_{latch} can be described below:

$$t_{latch} = \tau_{inv} \times \ln\left(\frac{V_{DD} - GND}{V_{idl}}\right) + \frac{K_{latch}}{(V_{DD} - V_{cm1} - V_{thp})^2} \tag{8}$$

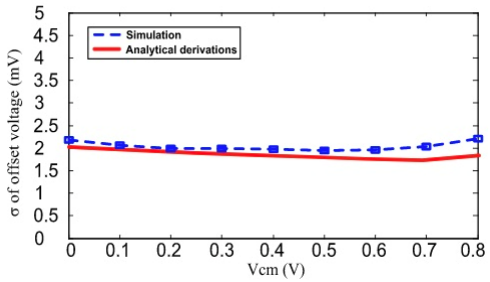


Figure 9. Offset voltage versus V_{cm}

The offset voltage depends on the V_{cm} because changes in the transistor operating region and non-ideal effects such as channel length manipulation change the effect of each component mismatch on the disparate gain.

$$V_{OS} = \frac{[g_m \Delta V_{th} + \Delta k(V_p - V_{th} - \Delta V_{th})^2 + 2V_{cm}\Delta k(V_p - V_{th} - \Delta V_{th})^2 - V_{cm}^2]}{(g_m - 2k\Delta V_{th} + \Delta k(V_p - V_{th} - \Delta V_{th})^2 - V_{cm})} + \frac{-\frac{\Delta\alpha}{2}(\frac{t_{amp}}{C})I}{(g_m - 2k\Delta V_{th} + \Delta k(V_p - V_{th} - \Delta V_{th})^2 - V_{cm})(1 + (\alpha + \frac{\Delta\alpha}{2})(\frac{t_{amp}}{C}))} \quad (9)$$

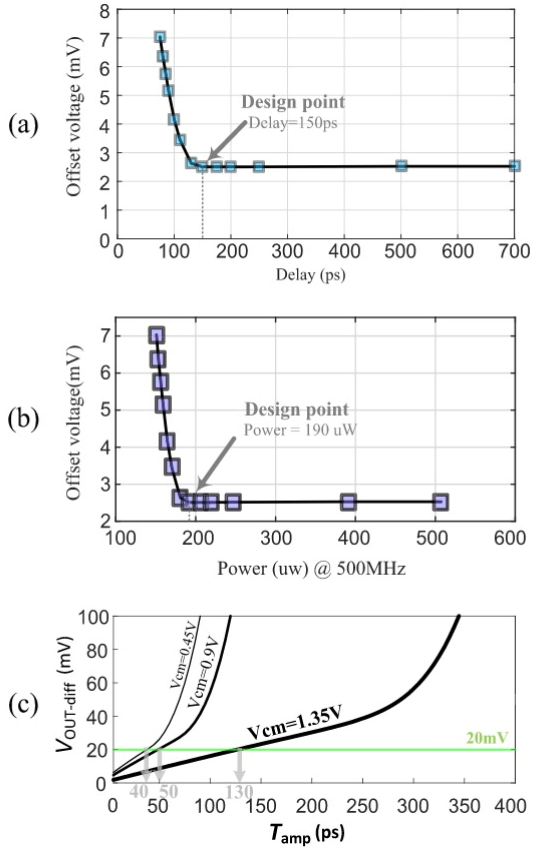


Figure 10. (a) Offset voltage versus delay (b) Offset voltage versus power(at 500MHz) (c) Offset voltage versus output differential voltage at t_{amp}

Figure 10 show the offset voltage of the proposed design with respect to the t_{amp}, and the power dissipation with respect to the power generated by different t_{amp} values. Clearly, t_{amp} = 150ps is the optimal design point.

The total power consumption is：

$$Power = \frac{1}{T}\int_0^{T=T_{clk/2}} v(t)\cdot i(t)dt + P_{latch}$$
$$= \frac{1}{T}\int_0^{t_{amp}} V_{DD}(I_1 + I_2)dt + P_{latch} \cong \frac{t_{amp}}{T} V_{DD} \times I_{M8} \quad (10)$$

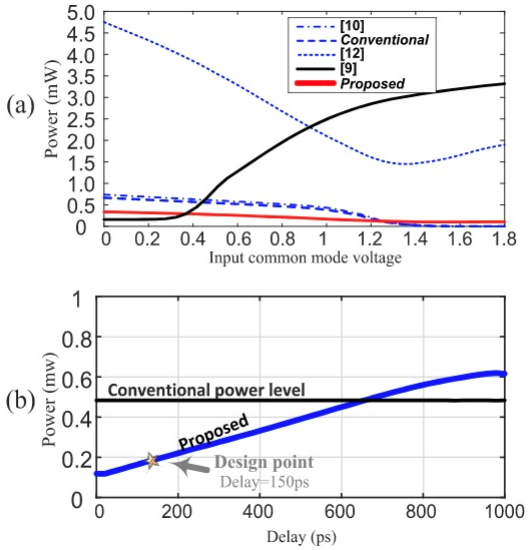


Figure 11. (a) Power consumption versus V_{cm}
(b) Power consumption versus t_{amp}

Figure 11(a) shows the power consumption versus V_{cm} at 500 MHz. When the input V_{cm} is low, the output voltage of the preamplifier fluctuates greatly. Therefore, if the latch's power consumption is ignored, the lower the V_{cm}, the higher the power consumption.

Figure 11(b) shows the relation between power consumption and delay when V_{cm} =1.1V. The traditional power level is settled because the preamplification delay is constant to T_{clk} /2. There is a linear relationship between power consumption and t_{amp} in the proposed comparator.

In this comparator, a pMOS latch and pMOS preamplifier are used along with a small cross-coupled circuit, and a particular clock mode is used to modify the preamplifier gain. Clock mode provides adequate preamplifier gain. Because the pMOS transistor is used at the latch's input, in order to maintain the common-mode voltage at a low level at the output of preamplifier, the cross-coupled circuit is utilized. Then, comparator's speed is improved and is consistently high over the wide range of input V_{cm}. So as to significantly reduce power consumption, we can invalidate the preamplifier after the optimal delay.

Therefore, the design is a low offset high rate low power comparator operating in broad common-mode voltage input extent. However, the input noise of the proposed design reaches the same level as that of the CDC. Therefore, the further study of the comparator should take the noise reduction into consideration.

2.3 The analysis of the EPC

This section introduces a novel energy-saving comparator based on ring oscillator collapse called edge pursuit comparator. The comparator voluntarily alters the comparison energy based on its input differences out of control, thus removing energy spent on coarse comparisons which is not necessary.

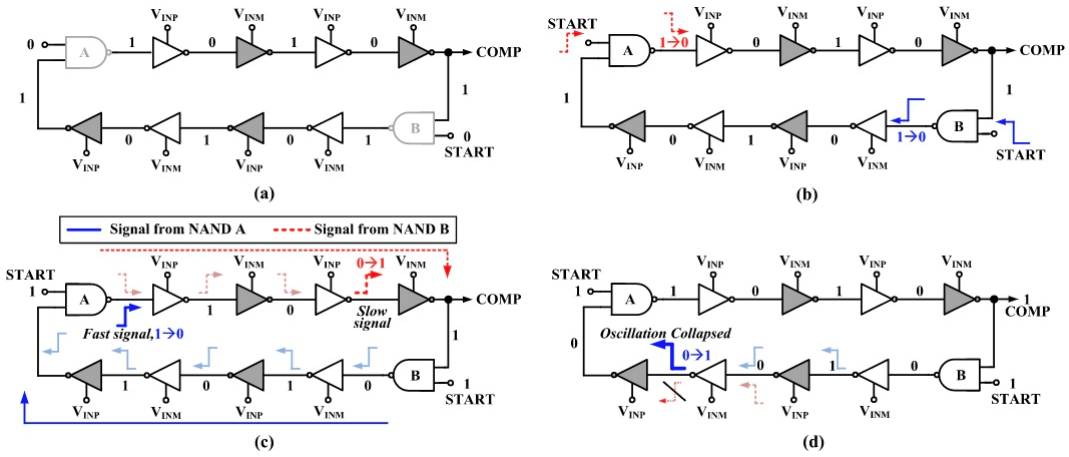


Figure 12. (a) Reset state (b) Intial stage of the Comparison
(c) Edge transmission (d) Termination of the Comparison

The structure of EPC is made up of two NAND gates and inverter delay units. Initially, we can see in Figure 12(a), the comparator is in resetting because signal START is low, which breaks the oscillating path. Once signal START at both NAND gates is high, the comparator starts the comparison [Figure 12(b)]. This will inject two propagation edges into the oscillator until one surpasses the other and the oscillation collapses [Figure 12(D)]. Also, the oscillator can move around the comparator [Figure 12(c)]

V_{INP} and V_{INM} which are the differential input signals are alternately used to the top and base current to limit transistors of the delay cell in order to modulate the pull-up and pull-down edge propagation delays. The incompatible current limiting transistors control the propagation delays of these two edges. Therefore, increasing V_{INP} or V_{INM} will cause one edge to get a quicker propagation and the other edge to get a slower one.

Once one propagating edge passes the other, as shown in Figure 13(a), the oscillations collapse and the stage output stabilizes to either V_{DD} or the ground, depending on which edge is slower, thus exceeding. If the voltage difference between V_{INP} and V_{INM} is subtle, as shown in the Figure 13(b), the two injection edges will have the cycles' number required to voluntarily make a decision to advance and resembled propagation delays. For large voltage differences, oscillations inherently collapse rapidly, limiting the dynamic energy consumption of coarse comparisons.

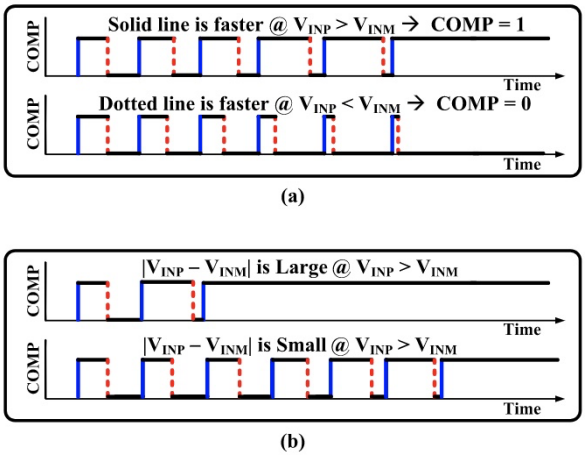


Figure 13. Output versus time

In comparison, EPC works like a ring oscillator. Once triggered, the two injected edges will propagate at different speeds with different transistor drives, and their phase differences will drift until they are shifted $-\pi$ or π compared to the beginning of the propagation. Therefore, the noise can be reckoned by studying the time domain or the phase difference, rather than by analyzing the voltage or current.

Then, in the phase domain, during a comparison, we can suppose that f(t) which means the phase difference is a continuous time random process which has independent increments in nonoverlapping time intervals.

And the solution to the system is:

$$f(t,\phi)=\frac{1}{\pi}e^{\frac{M}{\Sigma}\phi}\sum_{n=1}^{\infty}e^{-\lambda(n)t}\cos(k(n)\phi) \tag{11}$$

In the formula above, the "drift" and "diffusion" coefficients are represented as M and ∑:

$$\begin{aligned} M&=\frac{\mu_{\Delta\phi}}{\tau}=4\pi f_0\frac{v_{in}}{V_{ov}}\\ \Sigma&\equiv\frac{\sigma_{\Delta\phi}^2}{\tau}=8\pi^2 f_0^2\frac{kT}{I}\left(\frac{2}{V_{ov}}(\gamma_N+\gamma_P)+\frac{2}{V_{DD}}\right)\end{aligned} \tag{12}$$

With taking the derivative with respect to t, we can get the probability density function of T:

$$\begin{aligned} f_T(t)&=\frac{d}{dt}P[T\le t]=-f'(t)=\frac{1}{\pi}\Sigma\cosh\left(\frac{M}{\Sigma}\pi\right)\\ &\times\sum_{n=1}^{\infty}(-1)^{n+1}k(n)^{-\lambda(n)t}\end{aligned} \tag{13}$$

Therefore, medial comparison time E[T] is:

$$E[T]=\int_0^{\infty}tf_T(t)dt=\frac{\pi\tanh\left(\frac{M}{\Sigma}\pi\right)}{M}=\frac{\pi^2}{\Sigma}S\left(\frac{M}{\Sigma}\right) \tag{14}$$

Where S is the scaling factor, which depends on the ratio M/∑:

$$S(k)\equiv\frac{\tanh(k\pi)}{k\pi} \tag{15}$$

Then, the average energy consumption needed to one comparison can be described as:

$$E=P\times E[T]=2IV_{DD}\frac{\pi^2}{\Sigma}S\left(\frac{M}{\Sigma}\right) \tag{16}$$

Taking the formula and the parameters into account, we can see the E is inversely proportional to f_0 and positively related to tan $h(I/f_0)$.

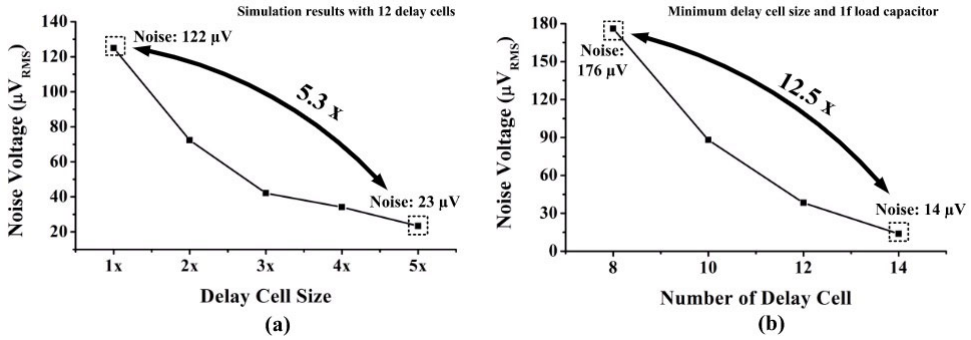


Figure 14. (a) Noise voltage versus delay cell size
(b) Noise voltage versus delay cell number

A random variable v_n which is the comparator's input-referred noise has a probability density function $f_{vn}(v)$ which meets:

$$h(v_{in})=\int_{-\infty}^{\infty}H(v_{in}+v_n)f_{v_n}(v_n)dv_n=\int_{-v_{in}}^{\infty}f_{v_n}(v_n)dv_n \tag{17}$$

Then, the input-referred noise power σ^2 v_n is:

$$\sigma_{v_n}^2 = \int_{-\infty}^{\infty} v_n^2 f_{v_n}(v_n) dv_n = \int_{-\infty}^{\infty} v_n^2 h'(v_n) dv_n$$
$$= \frac{\pi^2}{3} f_0^2 (\frac{kT}{I})^2 (\frac{2}{V_{ov}}(\gamma_N + \gamma_p) + \frac{2}{V_{DD}})^2 V_{ov}^2 \quad (18)$$

Therefore, the noise RMS level is:

$$\sigma_{v_n} = \sqrt{\sigma_{v_n}}^2 = \frac{\pi}{\sqrt{3}} f_0 \frac{kT}{I} (\frac{2}{V_{ov}}(\gamma_N + \gamma_p) + \frac{2}{V_{DD}}) V_{ov} \quad (19)$$

According to (19), we can see that the RMS rank is directly proportional to f_0/I. This feature makes it easy to tune the required input reference noise levels for this comparator topology over a wide range at design time and runtime. Otherwise, instead of the RMS level, conventional comparators typically need adjustment of design factors that are inversely proportional to the requisite noise power, making it more difficult for wide-range noise adjustment. As shown in Figure 14(a), with transforming the overall capacitance by modifying the size of each inverter unit, the noise RMS rank haply conforms the inverse of the all capacitance.

We can see in Figure 14(b), another one attempts to adjust the total capacitance by varying the delay units' number. But simulation results manifest that the noise alters more susceptibly than expected because of the positive feedback phase difference shift. We can see from the Figure, this positive feedback affects comparators with fewer series more because of the shorter reset time. This method is resembled as the output signal regeneration of a conventional comparator, but it costs little energy in this phase regeneration, whereas the voltage regeneration of a traditional comparator costs a settled sum of dynamic energy. Therefore, the energy efficiency of EPC can be kept with only a small number of stages. Such positive feedback method greatly broadens the tunable noise range.

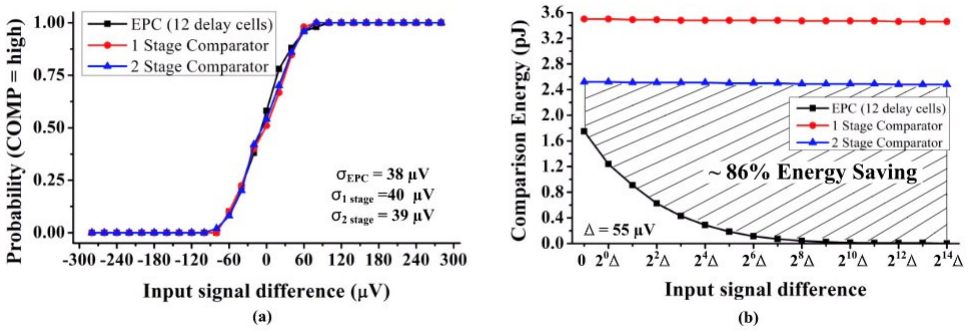


Figure 15. Comparison of comparator performances (a) Probability for output "high" (b) Energy during comparing versus input signal difference

The energy scaling factor S(M/∑) is a great factor contributes to the EPC's energy consumption. For the sake of estimating how much energy is saved, we need to obtain the relationship between M/∑:

$$\frac{M}{\Sigma} = \frac{1}{\sqrt{12}} \frac{v_{in}}{\sigma_{v_n}} \quad (20)$$

For estimating the EPC's energy efficiency and comparing, we need to delimit a standard for comparing:

$$\begin{aligned} N &\equiv E \times \frac{\sigma_{v_n}^2}{V_{DD}^2} \\ N_{EPC} &\cong \frac{\pi^2}{3} S(\frac{M}{\Sigma}) kT\gamma \frac{V_{ov}}{V_{DD}} \\ N_{SS} &= E_{SS} \times \frac{\sigma_{v_n ss}^2}{V_{DD}^2} \cong 4kT\gamma(1+\frac{3C_O}{4C_X})\frac{V_{ov}}{V_{th}} \\ N_{TS} &= E_{TS} \times \frac{\sigma_{v_n Ts}^2}{V_{DD}^2} = 4kT\gamma \frac{V_{ov}}{V_{th}} \end{aligned} \tag{21}$$

The ratios of these guidelines are as follows:

$$N_{EPC} : N_{SS} : N_{TS} = S(\frac{A}{B})\frac{\pi^2/3}{V_{DD}} : \frac{7}{V_{th}} : \frac{4}{V_{th}} \tag{22}$$

Figure 15 shows three comparator comparisons' simulation results. With resembled input referred noise levels, EPC represents substantial energy sparing from voluntary energy scaling. The other two comparators show almost equivalent energy dissipation. As shown in Figure 15(b), when V_{ov} is resembled as all the comparator types considered. The results are consistent with the tendency of (22).

The MOSFET mismatch causes the input reference offset voltage V_{OS} and makes each delay cell produce a small delay difference Dtd. Due to the mismatch factors in the delay units are not correlated, the standard deviation of the cumulative delay difference is $\sqrt{N}\cdot$Dtd when the edge runs the N-level delay unit for one lap. The N-stage delay cell's voltage-time gain ratio is $N\cdot Dtd/V_{OS}$, so the N-stage delay cell's V_{OS_N} which means the input referred offset voltage is:

$$V_{OS_N} = \frac{1}{\sqrt{N}} \cdot V_{OS} \tag{23}$$

With modifying the comparison energy, the design can eliminate energy spent on coarse comparisons which is not necessary. Therefore, the designed topography can reach a great amount of energy saving about 86%.

3. Conclusions

This paper analyzed two improved designs. The first one modified the circuit of a traditional double tailed comparator to reach low-power and quick operation. The positive feedback in the stage of regeneration is improved and the delay is greatly reduced. The other one is a low-power comparator. We can activate its latch delayed to avoid excess power consumption and get enough preamplification gain at the evaluation phase.

A novel design named EPC is also analyzed. By modifying the comparison energy on the basis of its input difference out of control, the comparator can automatically adjust the performance. Also, it can eliminate energy spent on coarse comparisons which is not necessary. Therefore, the designed topography can reach a great amount of energy saving about 86%. But the design doesn't take the delay into consideration. These deficiencies are our future improvement direction and focus of work.

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