A Novel Design Method for 4-bit Absolute-Value Detector

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Abstract: The wide use of comparator reinforces its improvements and innovations. For seeking a breakthrough, a 4-Bit Absolute-value Detector is studied and constructed. Different from common designs, this new version adds an absolute value converter using truth table. Owing to the participation of absolute value detector the comparator can compare the absolute value of the two inputs' value directly in this detector. Furthermore, the detector’s delay and energy consumption which are calculated by critical path data demonstrates the performance of the detector and provides circuit optimization scheme indirectly. The analysis indicates that this improved version's minimum and maximum delay is 50.556 and 75.834 and energy consumption is 39.8% lower when supplied by optimal VDD than 1V VDD. Combining the converter with the comparator, a 4-Bit Absolute-value Detector model with smaller size and higher efficiency is built.

Keywords: Comparator, Detector, Path-effort.

1. Introduction

A comparator [1] in circuit can compare two input value. For instance, the application of comparator is very extensive, and comparators sometimes play an extremely important role in some situation such as comparing two input signals, judging whether the input signal passes the preset value and selecting the best input. Due to the wide use of comparator, its importance causes demand for comparator with faster processing speed, smaller size, and better security. Recently, elements, voltage, and other relevant parameters have been confirmed they affects the performance of the comparator [2].

Considering the influence of structure, this paper provides a new converter design circuit diagram which has fewer logic gates is designed by the formulas of the circuit conducted by the truth table. This absolute value converter removes the signal bit of one input to ensure this input is 3-bit and it is always positive. Therefore, the converter only needs to convert the other input to a positive value.

Because of the participate of the absolute value converter, the comparator omits the comparison of signal bit and compares two inputs’ 3-bit value. When there occurs a larger one during the comparison process of bits, it means the larger one has higher value. To reflect performance of the circuit and help optimize the circuit, this paper purposes a method that making use of critical path to analyse the minimum path and calculate the minimum path delay.

Besides, taking advantage of optimal V_{DD} helps figure out the maximum path delay and energy consumption. The three parameters are slightly higher, and the circuit size is smaller, which reveals optimizations of this circuit design. This paper describes the design and system considerations of the 4-Bit Absolute-value Detector.

The paper is organized as follows. Section 2 presents the circuit diagram and the implementation of the converter and comparator. The circuit analysis is discussed in Section 3. Section 4 shows the optimized design, and Section 5 summaries the results. Finally, Section 6 concludes the paper.

2. Circuit Implementation

This part mainly introduces how the whole circuit is built. The absolute value detector is the circuit comparing the two inputs' absolute values. Based on this purpose, the main function can be separated

into two parts. The first function aims to find the absolute value of one of the inputs, input A. The second function is designed to compare the absolute value of input A, with input B.

2.1. Absolute Value Converter

Basically, the circuit is built based on their formulas, the truth table, or the K map. Among most absolute value converter designs, the circuit diagram is used 2's complementary formula to convert the negative number and it can be seen in Figure 1.

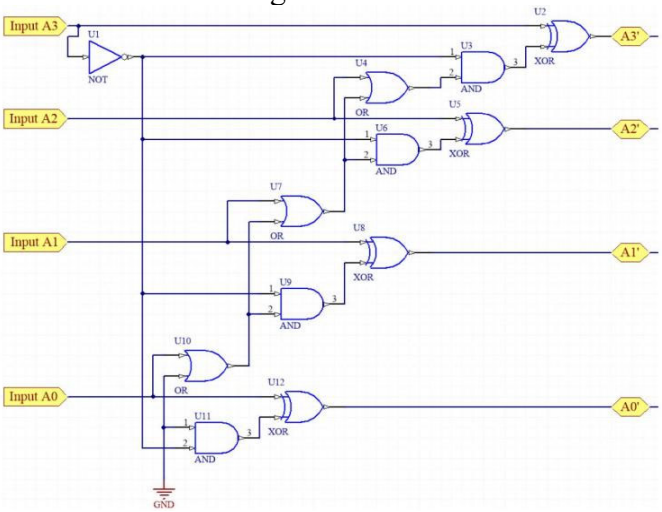


Figure 1. Normal Converter Diagram. [3]

In this paper, the formulas of the circuit are conducted by the truth table. This new circuit is presented in Figure 2. In this case, fewer transmission gates of the converter are used to build instead of the normal ones. The following diagram shows how to build the circuit.

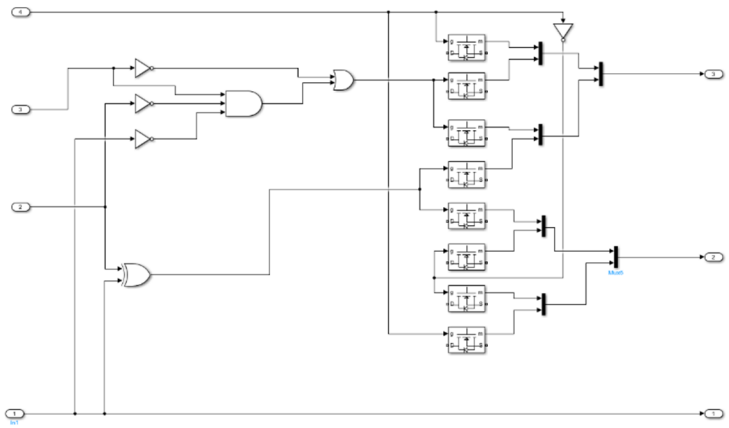


Figure 2. Converter Design Circuit Diagram.

2.2. Comparator

For the comparator, the circuit diagram is mostly followed the common principle: the value of higher bits is larger than that of the lower bits, and the larger value of the whole number will be. This is what the diagram shows in Figure 3.

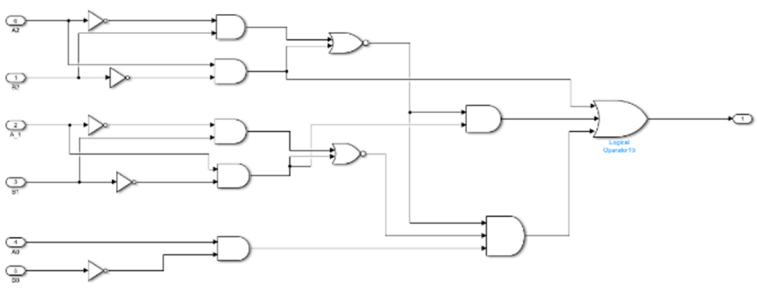


Figure 3. Comparator Design Circuit Diagram. [4]

2.3. Whole Circuit

Based on the two parts before, the whole circuit is simply combined by these two parts. This is how the whole circuit is presented as:

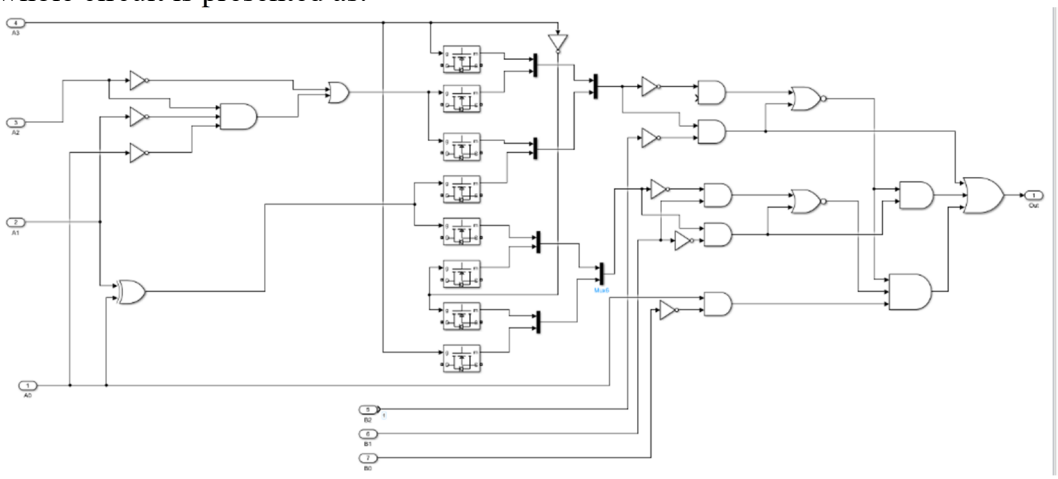


Figure 4. Whole Circuit Diagram

3. Circuit Analysis

This part is mainly about how the circuit works in the diagram—followed by the sequences of the Circuit Implementation.

3.1. Absolute Value Converter

According to the input type definition, the inputs are quite different. One of the inputs, input A, is a 4-bit number in the 2's complement number. 2's complement number has the signed bit as the most significant bit and the last three are the actual value of the input. However, unlike normal signed numbers, 2's complement number has its own method to represent the negative number. The other input, input B, is only 3-bit and it is always positive. As a result, the only input that needs to convert is input A. There are two scenarios when input A appears.

(1) When the input is a positive number, the absolute value converter should output the origin value. In another word, the absolute value converter should either be 'not working' at all or choose the original value instead of the value after the inverter.

(2) When the input is a negative number, the absolute value converter should output the value after converting. To convert the negative number, 2's complementary number has its own formula.

$$|A| = (\bar{A} + 0 \times 01) \quad (1)$$

Mostly the circuit is built by implementing this formula into the actual circuit. Parallel to the positive input which doesn't need to be converted, there is one way to convert the negative number. Instructed by the formula, an inverter and a carry adder are in series. Besides the inverter, a 'full adder' should be added. Like the full adder, it should take into account the carry between every bit.

Table 1. Truth table of the absolute value converter.

A3	A2	A1	A0	A2'	A1'	A0'
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	1	0	0

0	1	0	1	1	0	1
0	1	1	0	1	1	0
0	1	1	1	1	1	1
1	1	1	1	0	0	1
1	1	1	0	0	1	0
1	1	0	1	0	1	1
1	1	0	0	1	0	0
1	0	1	1	1	0	1
1	0	1	0	1	1	0
1	0	0	1	1	1	1
Formula				$\overline{A3}A2 + A3\overline{A2} + A3A2\overline{A1A0}$	$\overline{A3}A1 + A3(A1XORA0)$	A0

However, implementing this formula means adding an inverter to every bit and building an adder for the whole circuit. By contrast, by listing all the input and the output, every bit would have its unique formula to implement. It might decrease the number of irrelevant electrical components. To figure out whether the truth table can help to minimize the delay of the circuit, the team builds the truth table below and find the relationship between the input and the output.

Based on the Table 1 above, each bit has its own principle for converting the negative number. Compared with the formula of the 2's complementary, this method seems to consume more gates. However, unlike the formula for converting the 2's complementary number, this formula also includes the situation when the input is positive. In another word, for the previous circuit design, when including the positive number, more logic gates are needed than the truth table method. It also performs better in the area of delaying, which will be determined in the paragraphs below. Here is how the circuit is implemented by the truth table.

3.2. Comparator

Once input A is converted to the 3-bit positive value, the final result of the circuit is whether input A is higher than input B. Unlike the decimal comparison, the method to compare in the circuit is quite complicated. Since the circuit could only distinguish the higher value of two single bits, it is quite necessary to take into account how the decimal number is compared.

For two decimal numbers, the higher bit at the more significant position will make the whole number bigger than the other number, no matter whether other bits are less significant position. Based on that theory, the MSB should be compared first. The less significant bits should be taken into account if and only if the more significant bits are equal. With this conception, relative formulas are written.

$$F = A2\overline{B2} + x2A1\overline{B1} + x2x1A0\overline{B0} \quad (2)$$

$$x2 = A2B2 + \overline{A2B2} \quad (3)$$

$$x1 = A1B1 + \overline{A1B1} \quad (4)$$

According to the formulas above, the whole circuit is built.

4. Sizing Optimization of Critical Path

4.1. Determine the critical path

The concept of the critical path is given in [5]. As analyzed, the first critical path [6] is listed in the following Figure 5.

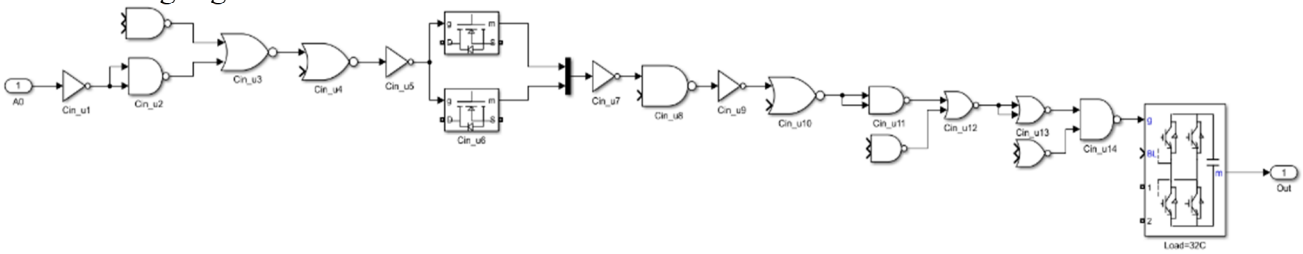


Figure 5. Critical Path Determination.

4.2. Minimum Path Delay

Table 2. Specifics in circuit design.

Gate Type	Number of Inputs				
	1	2	3	4	n
inverter	1				
NAND		4/3	5/3	6/3	$(n+2)/3$
NOR		5/3	7/3	9/3	$(2n+1)/3$
Trisate, multiplexer	2	2	2	2	2
XOR, XNOR		4,4	6,12,6	8,16,16,8	

From the critical path diagram [7] showed in Figure 5, C_{inu} indicates the size of the gate, which is expressed as:$g \bullet \frac{C_{out}}{f^*}$; In the following calculations regarding the minimum path delay, Path Effort indicates the delay of the path, G indicates the total path logical effort, B here indicates the total path branching effort, and H means the total path electrical effort. In this critical path:$G = \prod g_i = \frac{1.6\times10^6}{3^9}$; H means the path electrical effort:$H_{path} = C_{out}/C_{in}$; C_{inu} stands for the size of the gate; D_{min} means the minimum path delay [8], which is calculated as= $\sum(g_i h_i) = Nf^* + P$; N stands for the number of stages: which is 14; P stands for the Parasitic delay of the critical path; And, f^* is the optimal stage effort, which is calculated as :$f^* = \sqrt[n]{Path\ Effort}$. The design specifics are shown in Table 2.

$$H_{path} = \frac{C_{out}}{C_{in}} = 32 \tag{5}$$

$$PathEffort = \frac{1.6\times10^6}{3^9} \times 32 \tag{6}$$

$$C_{in} = g \bullet \frac{C_{out}}{f^*} \tag{7}$$

$$\mathrm{B} = 1 \tag{8}$$

$$f^* = (Path\ Effort)^{\frac{1}{n}} = 1.754 \tag{9}$$

$$\mathrm{P} = 26 \tag{10}$$

$$D_{min} = \sum(g_i \times h_i) = N \times f^* + P = 50.556 \tag{11}$$

Through calculation, here are the sizes of each component:

$$C_{inu10} = 15.87, C_{inu9} = 9.05, C_{inu8} = 6.88, C_{inu7} = 3.92, \tag{12}$$

$$C_{inu6} = 4.77, C_{inu5} = 2.55, C_{inu4} = 2.42, C_{inu3} = 2.30, \tag{13}$$

$$C_{inu2} = 1.75, C_{inu1} = 1 \quad (14)$$

4.3. Optimal V_{DD} supply

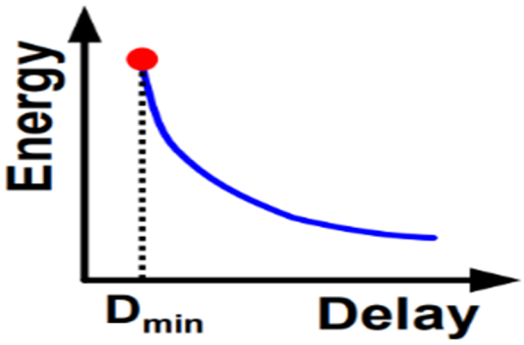


Figure 6. Relationship between Delay and Energy [9]

As the diagram indicates that at minimum delay, the energy consumption is too high and thus not cost-efficient. The optimization of V_{DD} is to figure out a supply voltage that has a low energy consumption while does not significantly increase the delay.

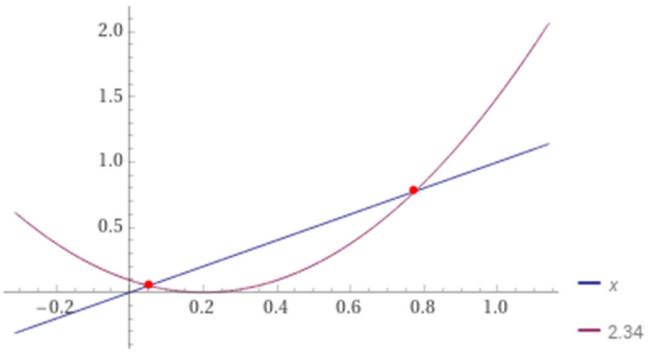


Figure 7. Relationship between V_{DD} and D

$$D \propto \frac{V_{DD}}{(V_{DD}-0.2)^2} \quad (15)$$

When $V_{DD} = 1V$

$$D \propto \frac{1}{(1-0.2)^2} \quad (16)$$

When V_{DD} is at its optimal, assume it is x in Figure 7.

The diagram here indicates that there are two possible solutions for V_{DD} supply. And, it is assumed that the maximum delay occurs at optimal V_{DD}. Though the lower one has a significant advantage over the higher one, it is much lower than the transistor's threshold voltage, 0.2V. Thus, to enable the transistor, the optimal V_{DD} is set to 0.776V.

When $V_{DD} = 0.776V$

$$D' = 1.5D_{min} = 75.834 \quad (17)$$

Energy Consumption when V_{DD} is 1V

$$E = C_{path} \times \dot{V}_{DD}^2 = 136.63 \quad (18)$$

Energy Consumption at optimal V_{DD}

$$E = C_{path}\left(\dot{V}_{DD}^{opt}\right)^2 = 82.28 \quad (19)$$

Upon calculation, the energy consumption drops around 39.8 percent [10] when supplied with optimal V_{DD}, though the delay is one and a half of the minimum delay.

4.4. Effects on the delay of non-critical path

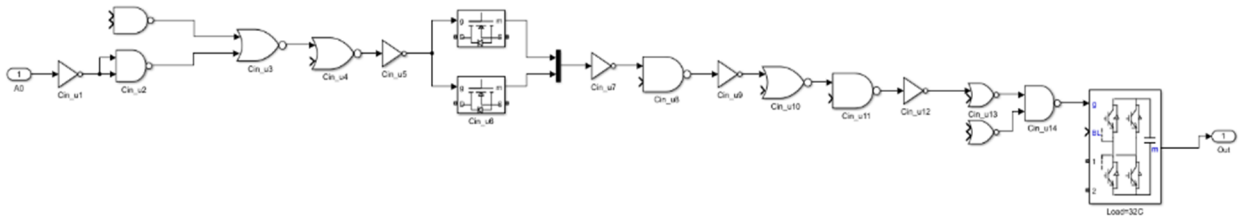


Figure 8. Non-critical path A

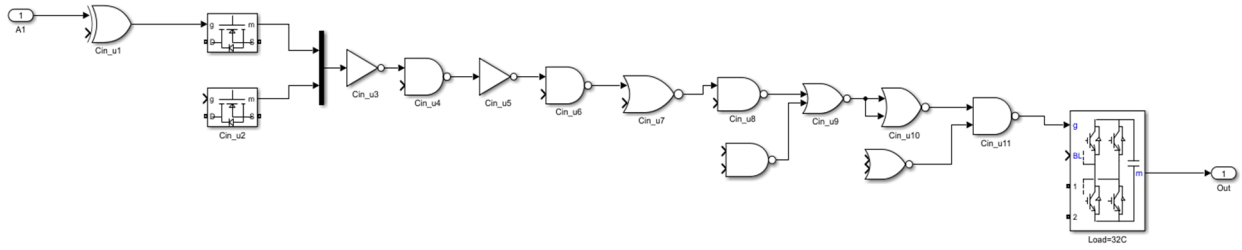


Figure 9. Non-critical path B

Non-critical paths A and B are the second and third longest paths except the critical path. The delay for Noncritical path A is 48.66 and 47.21 for B respectively, which are both smaller than the delay of the critical path, 50.556.

5. Summary of circuit configurations, delay calculations, and energy consumption

5.1. Circuit topology and sizes

The circuit is built mostly based on the basic conception of the 2's complementary number. Besides the basic conception, the truth table is used to optimize the whole circuit in order to minimize the delay.

Upon sizing optimization, the total capacitance of the critical path is 136.63, with 14 different sizes. Compared the sizes to those of the Paper: Improved Design of a 4-bit Absolute-Value Detector Using Simplified Chain Carry Adder, the total size is larger except some of the components are not as large as those in the Paper.

5.2. Delay calculation

Upon calculation, the sizes of different components in the critical path have been determined. Then, the minimum delay of the critical path is figured out per the delay formula listed previously, which is 50.556. The maximum delay is also determined in the V_{DD} optimization part, which is one and a half of the minimum delay, 75.834. The minimum delay and the maximum delay in this design are both higher than those in the Paper: Improved Design of a 4-bit Absolute-Value Detector Using Simplified Chain Carry Adder.

5.3. Energy Consumption

After finishing the V_{DD} optimization, the energy consumption of the critical path is figured out, which is 82.28, which is 39.8 percent lower than that under 1V V_{DD}. Though the delay increases by 50 percent, it's worth having the trade-off as long as the energy consumption decreases. The energy consumption in this design is much larger than that in the Paper: Improved Design of a 4-bit Absolute-Value Detector Using Simplified Chain Carry Adder. Partly because in this design, the capacitance of the entire critical path is taken into consideration. However, the Paper: Improved Design of a 4-bit Absolute-Value Detector Using Simplified Chain Carry Adder only considered the energy consumption at the load. Though the nominal energy consumption is larger than that of the Paper:

Improved Design of a 4-bit Absolute-Value Detector Using Simplified Chain Carry Adder, the percentage reduction in energy consumption after implementing V_{DD} optimization is similar, both are around 39.8 percent.

6. Conclusion

In this paper, a 4-Bit Absolute-value Detector is built. Pursuing a smaller scale with better performance, this paper proposes a main idea that combines a comparator with an absolute value converter using truth table. This circuit is designed based on the conception of the 2's complementary number. Considering speed and accuracy, the absolute value converter deals with inputs by using truth table because truth table can quickly list and compare all possible situations and ensure accuracy of the results. Owing to the procedure of taking absolute value, the comparator removes the comparison of signal bits to show higher processing speed.

After circuit design, the other key point is to calculate some data to evaluate this detector's performance. The path delay is a crucial parameter of circuits. Thus, after determining the critical path the minimum path delay is calculated to be 50.556 by using unique formula. The analysis of diagrams and formulas indicates a conclusion that maximum path delay occurs at optimal V_{DD}. According to this conclusion, the optimal V_{DD} is eventually set to 0.776V and the maximum path delay is calculated to be 75.834. Besides, energy consumption is 39.8% lower when supplied by optimal V_{DD} than 1V V_{DD}.

As a result, the truth table does show great performance, compared with the 2's complementary formulas, and the circuit's scale gets effective shrink. However, for the comparator part, it may be better by using the transmission gates. Through the transmission gates, the comparator's circuit will be simplified and the detector's performance may get further improvement. For the path delay, it is slightly higher than other advanced comparators. Thereby, the circuit still need to be improved to find a lower path delay. These problems are our future improvement direction and focus of work.

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