A Review of Comparators Inprovment Design

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Abstract: This paper reviews and analyzes the three proposed new comparators, as a indirection of future works. The first improved design is the pre-amplifier improved comparator that the input of the latch is changed to a PMOS transistor, and a pair of cross-coupled transistors are used in the preamplifier part to amplify the gain, which finally realizes the proposed circuit with better comparison speed, more less power dissipation. The switch separated latch comparator is another improved design that the latching stage with separate gate-biased cross-coupled transistors. Using this new transconductance-enhanced latching stage enables dramatic reductions in delay and power dissipation. The third type of comparator proposed is an innovative design. It adds a capacitor to the input tail current source of the preamplifier. Compared with the original Elzakker comparator, power dissipation has dropped by almost 50%.

Keywords: Comparators, High speed, Low energy dissipation.

1. Introduction

Comparators are widely used in the design of integrated circuits. As an important part in the design of digital-to-analog converters, low-power, high-speed, high-precision comparators have always been the key research goals. The article synthesizes three types of comparators designed by other scholars, discusses the three types of comparators, and draws conclusions.

A new form of comparator proposed in the first part is pre-amplifier improved comparator [1], compared with the traditional one, it differs by using PMOS transistors at the input of the preamplifier of the comparator and the latch stage, resulting in increased speed.

The second part propose a switch separated latch comparator [2], which based on the conventional two-stage dynamic comparator, using separate gate-biased cross-coupled transistors. Its advantage is that the switch is added in the latch part, so the parameter setting of the switch is analyzed in detail in this paper. The circuit thus achieves lower power dissipation and higher speed.

The dynamic bias comparator [3] is a good innovative design, and its design mentalities are discussed in detail later. The working principle of this comparator is to add a capacitor to the part of the preamplifier input tail current source, the source potential V_S has been stabilized, which makes the circuit working in a more constant state. The energy dissipation of the circuit has been significantly reduced, but the delay problem of this comparator has not been well resolved.

The paper is organized as follows. Section 2 describes the specific design principles of the three comparators, as well as parameter analysis. Section 3 concludes the paper.

2. The specific design of the proposed comparators

2.1 The pre-amplifier improved comparator

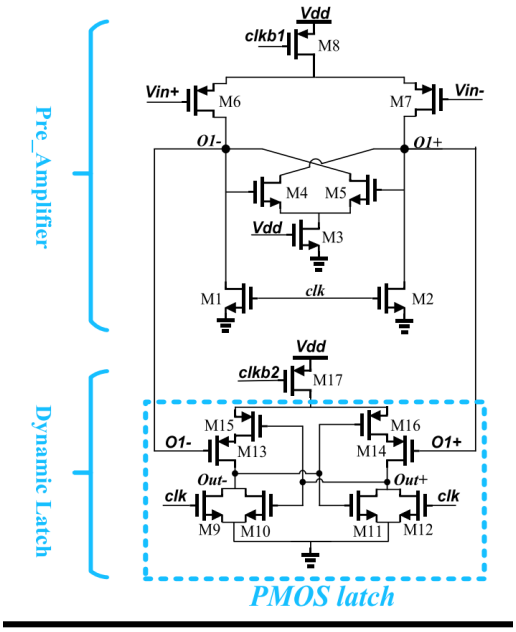


Figure 1. Proposed pre-amplifier improved comparator.

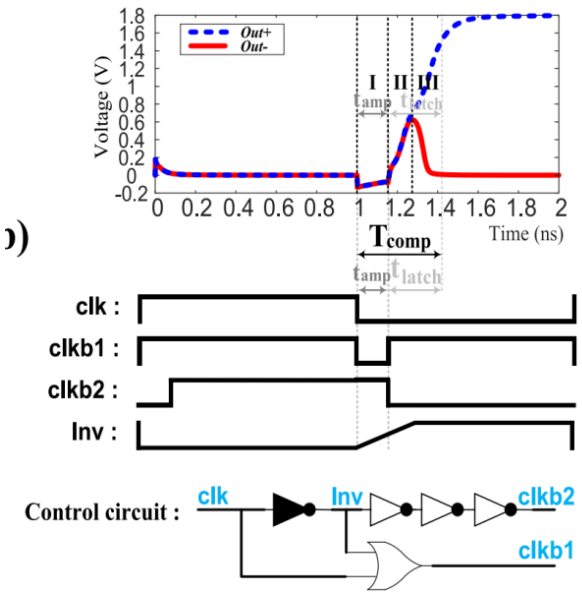


Figure 2. Its output waveform and clock signal.

A new form of comparator has been proposed as shown in Figure 1[1]. Compared with the traditional one, its difference is that the input terminals of the latch are PMOS transistors, and in the preamplifier part, a pair of cross-coupled tubes are used to amplify the gain.

The proposed comparator uses PMOS transistors at the input of the preamplifier and latch stage of the comparator. Both are controlled by the local clock generator. Refer to Figure 2, the parasitic capacitors of the O1+ and O1- nodes are differentially charged under the control of the clock signal, during the evaluation phase. At this stage, the operation of the cross-coupling circuit can slowly increase the differential voltage and cut down the common mode voltage, and delay the latch activation to achieve sufficient preamplification gain, which avoids excessive power dissipation. At the same time, the smaller cross-sampling transistor increases the gain of the preamplifier, reduces the common-mode input to the latch, and turns on the PMOS transistor at the input of the latch, thereby reducing the delay [4]. In order to ensure that the proposed comparator circuit can meet the design requirements, the mathematical modeling analysis of some data indicators is carried out. The formula for delay is expressed as

$$t_{latch} = \tau_{inv} \times \ln\left(\frac{VDD - GND}{V_{idl}}\right) + \frac{K_{latch}}{(VDD - V_{cml} - V_{thp})^2} \quad (1)$$

K_{latch} in the formula is a constant, so the common mode voltage should be small enough and keep it low, and the differential mode voltage could be as large as possible.

The offset voltage is expressed as follow, it can be obtained that the offset voltage depends on V_{CM}, and in order to makes it possible to eliminate the effect of the latch on the V_{OS}, the size of the input transistor should be large enough.

$$V_{OS} = \frac{\left[g_m\Delta V_{th} + \Delta k(V_p - V_{th} - \Delta V_{th})^2 + 2V_{cm}\Delta k(V_p - V_{th} - \Delta V_{th})^2 - V_{cm}^2\right]}{\left(g_m - 2k\Delta V_{th} + \Delta k(V_p - V_{th} - \Delta V_{th})^2 - V_{cm}\right)} + \frac{-\frac{\Delta\alpha}{2}\left(\frac{t_{amp}}{C}\right)I}{\left(g_m - 2k\Delta V_{th} + \Delta k(V_p - V_{th} - \Delta V_{th})^2 - V_{cm}\right)\left(1 + \left(\alpha + \frac{\Delta\alpha}{2}\right)\left(\frac{t_{amp}}{C}\right)\right)} \quad (2)$$

From the following simulation Figures, we can analyze the relationship between the offset voltage and several other design indicators.

Figure 3(a) shows the relationship between offset voltage and delay. It can be seen that when delay=150 ps, that is the best design point, the V_{OS} is the smallest, and the offset voltage at this time is also the optimal value. If the delay is less than 150 ps, the offset voltage will be too large. Figure 3 (b) is the relationship between offset voltage and power dissipation. Similarly, when the offset voltage is 2.5, the value of power dissipation is relatively small.

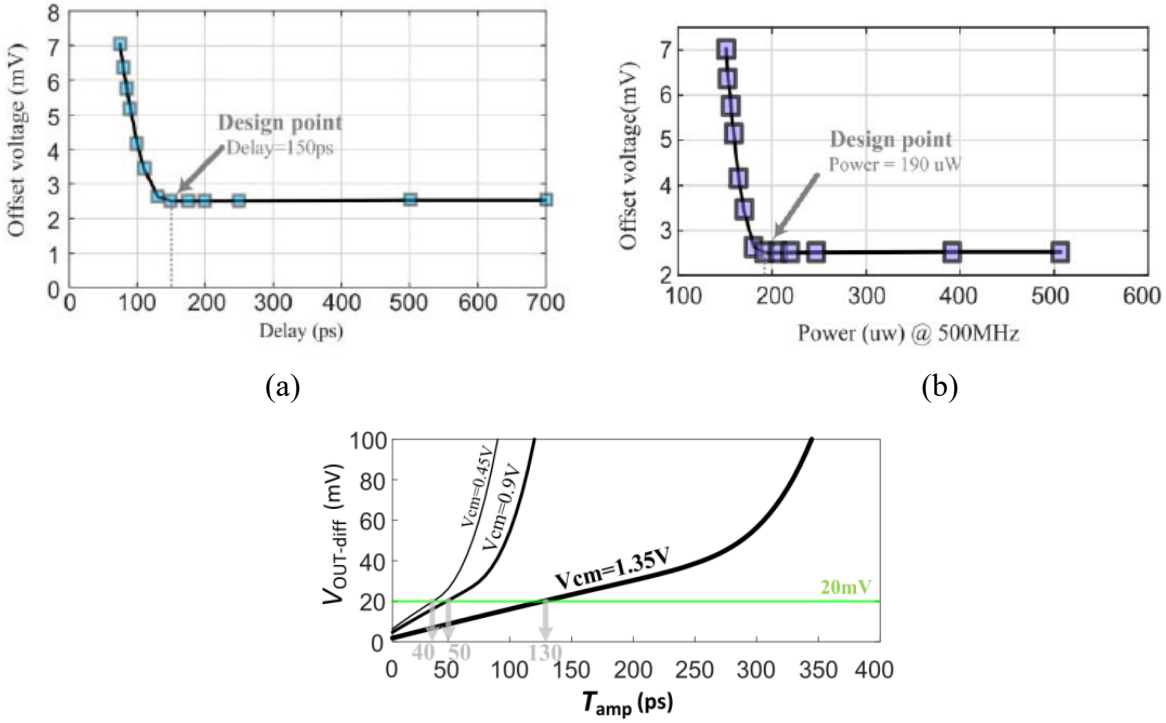


Figure 3. Comparison of V_{OS} with (a) delay and (b) power (c)$V_{OUT\text{-}diff}$ in preamplifier with t = t_{amp}.

It can be concluded in Figure 3(c) that the V_{CM} becomes larger, which will cause the delay to become larger as the differential mode output increases, and this circuit just drops the latch's common mode input, thus reducing the delay, so the value of V_{CM} is preferably less than 0.9mV.

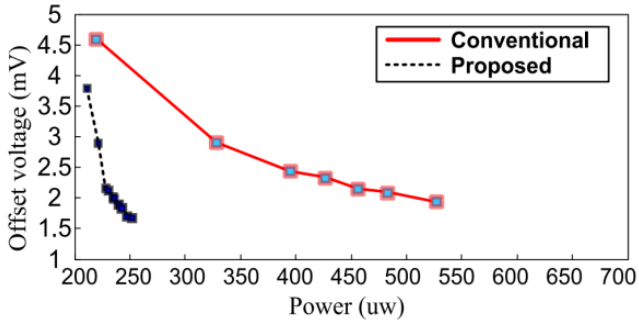
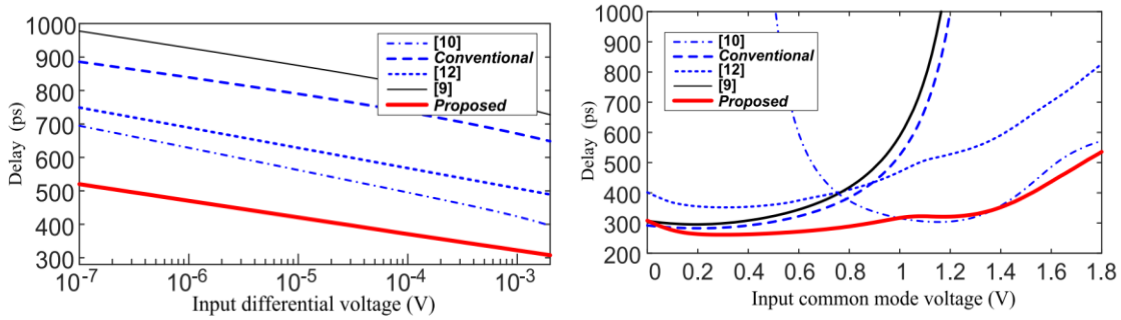


Figure 4. V_{OS} versus power dissipation of two comparators.

It can be seen from Figure 4 that the proposed comparator has a significant decrease in offset voltage and power dissipation compared with the traditional one.

For a more intuitive understanding of the optimization of the proposed comparator, some parameters of the design results are simulated and analyzed in this paper.



(a) (b)

Figure 5. (a) NMOS input and PMOS input comparator delay versus V_{id} simulation (V_{cm}=0.7,1.1). (b) Delay and V_{cm} simulation (V_{id}=1mV).

The relationship between differential mode voltage and delay, and common mode voltage and delay have been discussed in Figure 5. It can be clearly inferred that the proposed comparator is more than 150 ps faster than the other comparators when V_{cm} is 0.7V and 1.1V respectively. Assuming V_{id} = 1mV, the delay of the proposed comparator is the lowest and the most stable of all the simulated comparators.

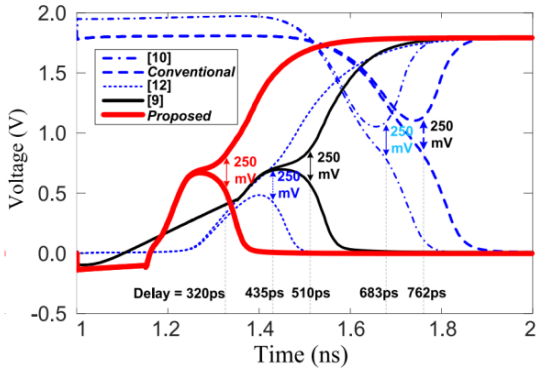
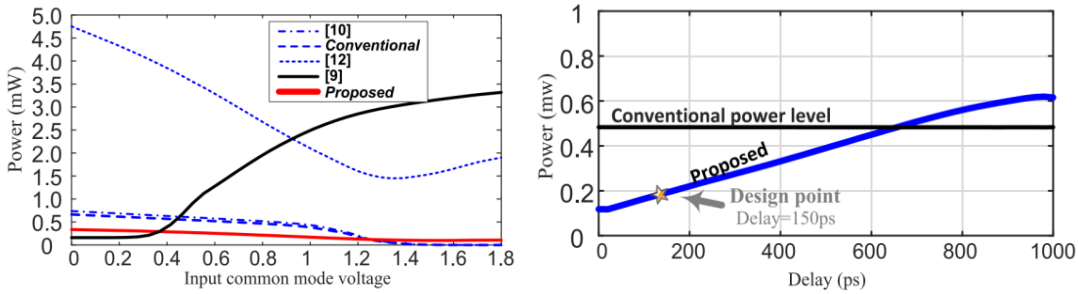


Figure 6. Simulation of the output waveform of the proposed, conventional, and some other comparators.

The output voltage of the comparator latch stage is shown in Figure 6, it can be concluded that the proposed circuit is faster than the others.



(a) (b)

Figure 7. (a)Simulated power dissipation and input V_{cm}. (b)Simolated power dissipation and t_{amp}, V_{cm}=1.1V.

As can be seen from Figure 7, the power consumption of the proposed comparator is basically the lowest among all comparators, and it tends to decrease with the increase of the input common mode voltage. In the proposed comparator, power dissipation is linear with delay. The advantage of this is when the delay of the new design is 150 ps, the power loss of the proposed comparator is much smaller than that of the traditional comparator. On the basis of t_{amp}=150 ps, the delay needs to be increased by 450ps, and the proposed comparator can achieve the same power dissipation as the conventional comparator.

Tests confirmed that, under the same conditions, the proposed circuit has 50% power reduction and 30% comparison speed is provided.

2.2 The switch separated latch comparator

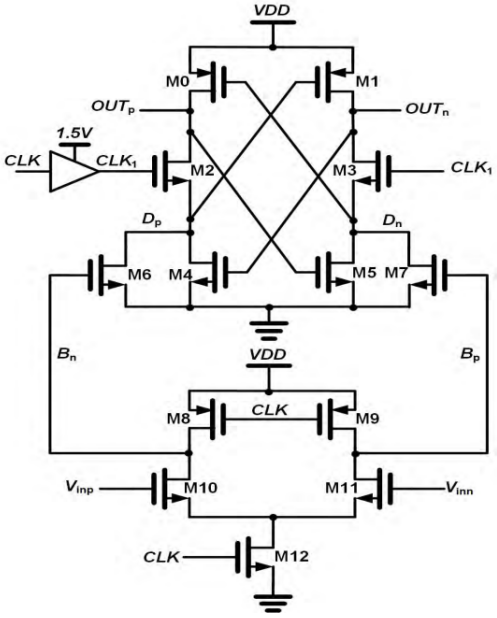


Figure 8. Schematic diagram of the proposed dynamic comparator.

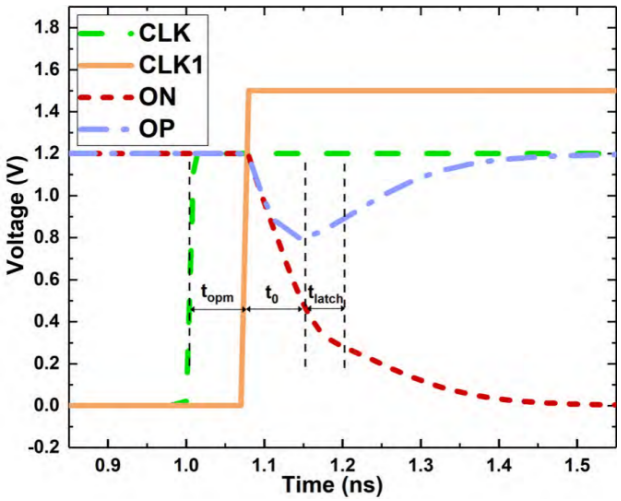


Figure 9. Typical waveforms of the proposed dynamic comparator

A new dynamic comparator [2] has the characteristics of low power dissipation and high speed, has a new latch stage is shown in Figure 8. The latching stage of proposed comparator employs transistors with separate gate-biased and cross-coupled. It achieves lower power dissipation and higher speed due to the increase in total effective transconductance during the comparison phase. Using this new method of switch controlling latch, delay and power dissipation can be greatly reduced.

Confirms in Figure 9, when CLK=0, it works in the reset stage, and the nodes OUTp and OUTn are charged to V_{DD} through M1 and M2 [5]. In addition, the metastable period of cross-coupled inverter is shorter because of the faster comparison speed, resulting in lower energy dissipation. The addition of CLK1 is to delay t_{opm} and make M2 and M3 open later, so as to minimize the short-circuit current of CLK rising edge through M6 and M7. In order to have a more intuitive display of the improvement of the latch part, the article modeled and analyzed the main design indicators. Formula modeling the delay of the proposed dynamic comparator is

$$t_{delay} = t_{opm} + t_0 + t_{latch} \tag{3}$$

$$t_{delay} = \frac{V_{THN} C_{OUT} \cdot 2\mu_p C_{OX} \frac{W_1}{L_1}}{g_{m,eff}^2} + \frac{C_{OUT}}{g_{m,eff}} \cdot \ln \frac{V_{DD}/2}{\Delta V_0} \tag{4}$$

Therefore, to optimize the delay of the circuit, the main parameter $g_{m,eff}$ should be as large as possible.

The latch's effective transconductance can be expressed as:

$$g_{m,eff} = g_{mn} + g_{mp} = \mu_n C_{OX} \left(\frac{W}{L}\right)_n V_{dsn} + \mu_p C_{OX} \left(\frac{W}{L}\right)_p |V_{dsp}| \tag{5}$$

It can be seen that $g_{m,eff}$ is related to the drain-source voltage of the latch transistor.

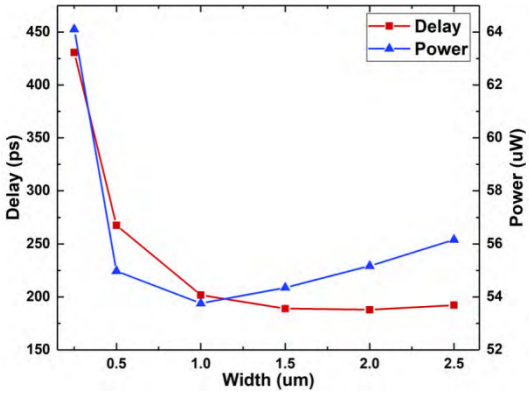


Figure 10. Simulated gm, eff of the conventional and proposed comparators.

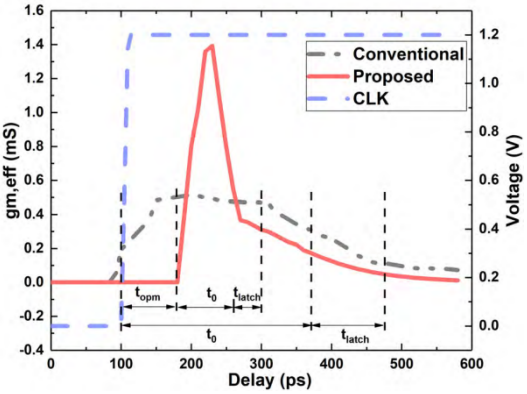


Figure 11. The delay and power dissipation versus the width of switches M2 and M3 of the proposed comparator.

Figure 10 concludes that the transconductance of the proposed comparator grows much faster than the other one, and the maximum value is increased nearly three times, so the proposed dynamic comparator has faster comparison and lower energy dissipation.

When designing this proposed comparator, some factors should also be considered. M2 and M3 in the circuit play the role of switches here, and the switches are turned on during the comparison phase, so that the output node can be fully discharged. Figure 11 expresses the analog power dissipation and delay of the comparator for different width switches. With the increase of the width, the delay shows a downward trend as a whole, but while the width of M2 and M3 is greater than 1um, the delay can't be reduced significantly by increasing the width, but also give rise to more power dissipation [6]. Hence the optimal width of M2 and M3 should be designed to be 1um.

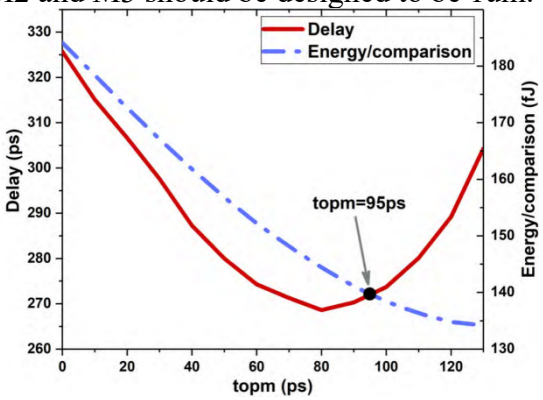


Figure 12. Simulation of delay and energy dissipation under different t_{opm} value.

It is obviously in Figure 12 that with the increase of t_{opm}, both delay and power dissipation tend to decrease. The delay is at the lowest point when t_{opm}=80ps, and then starts to rise again [7]. The position of the intersection of the two function curves is selected as the optimal design value, that is, when t_{opm}=95ps. The purpose of taking this point is to meet the minimum energy dissipation and delay.

Then the article conducts a simulation test on the designed comparator.

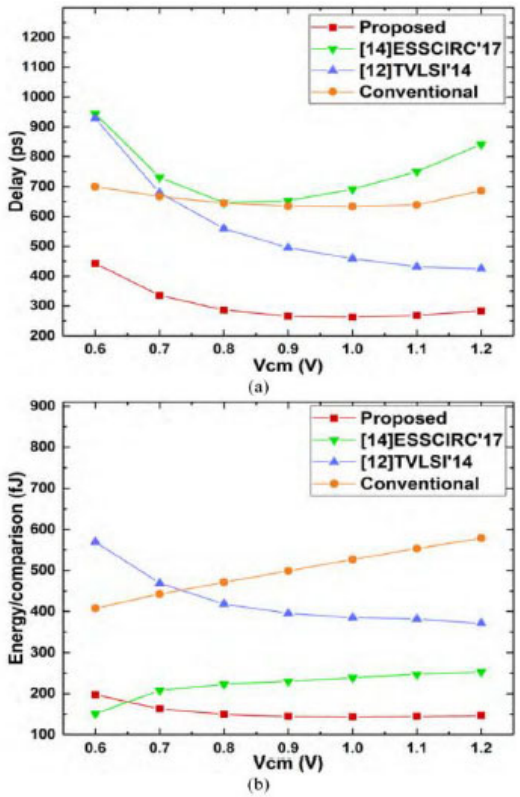


Figure 13. Simulation of (a) delay and (b) energy dissipation under different V_{cm}.

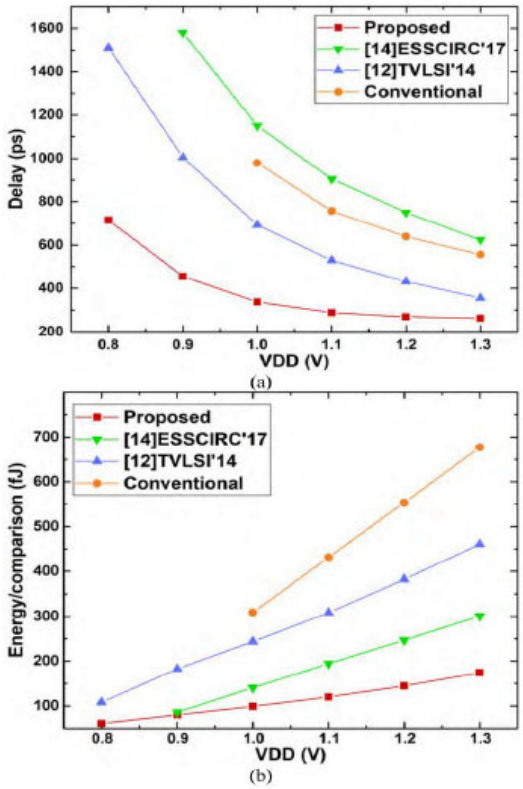


Figure 14. Simulation of (a) delay and (b) energy dissipation under different V_{DD}.

Figure 13 is the simulation between delay and energy dissipation and V_{CM}, which proves that the proposed comparator has much lower energy dissipation and delay than other types of comparators. It is at least 150ps faster than other comparators, and the energy dissipation is only 30% of traditional comparators.

Figure 14 is shown that, compared with the other three structures, the proposed dynamic comparator has significantly lower delay and energy dissipation in low voltage power supply, it is more suitable than other structures to work in low voltage, low power applications.

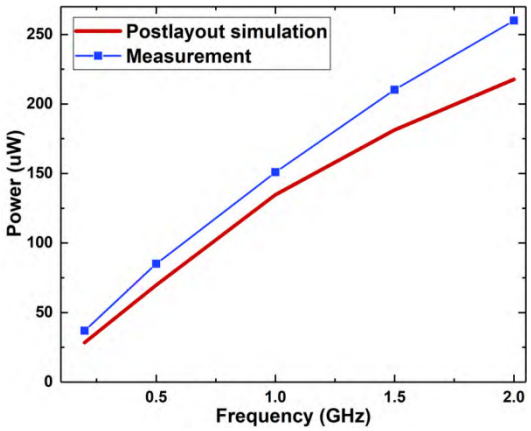


Figure 15. Simulation of power dissipation and operating frequency.

It can be obtained from the relationship between operating frequency and power dissipation in Figure 15 that the proposed comparator maintains low power dissipation at different operating frequencies, and the experimental results are basically consistent with the simulation.

So far, this dynamic comparator of locked-stage transconductance enhancement achieves the following, can work with low ground source voltage, has the characteristics of low power, high speed, and significantly reduces the delay and power dissipation.

2.3 The switch separated latch comparator

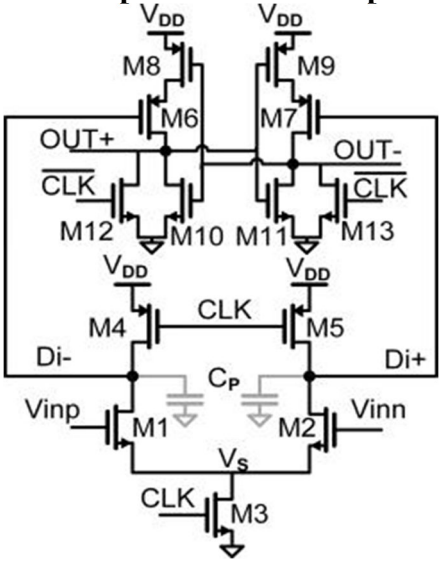


Figure 16. The Elzakker's comparator

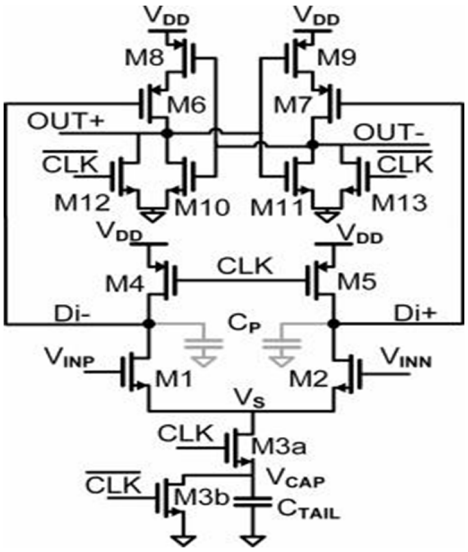


Figure 17. The dynamic bias comparator

The circuit in Figure 16 is the Elzakker's comparator, which uses the preamplifier and the latch in cascade. However, what we want to focus on is a new comparator is proposed as shown in Figure 17 [3] which is on the basis of the Elzakker's comparator, in order to optimize the power dissipation.

Its working principle is that a capacitor is added to the input tail current source of the preamplifier. After the capacitor is charged, the charge of the upper-level board remains constant, so V_S is constant, and the difference between the gate terminal potential and the source terminal potential is unchanged. Therefore, the static operating point of the common mode remains stable, so that the working state of the circuit is more stable, there is no frequent charging and discharging, and the power dissipation is reduced [8]. From the results in Figure 18 and Figure 19, it can be inferred that the common mode input and voltage gain of the preamplifier have been significantly improved.

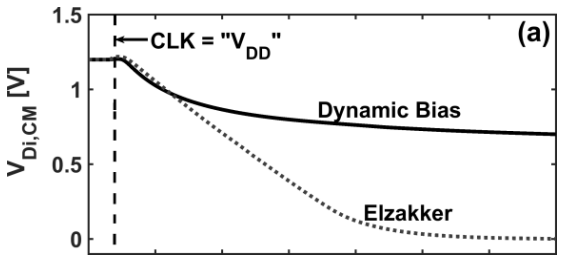


Figure 18 Common Mode Voltage Comparison.

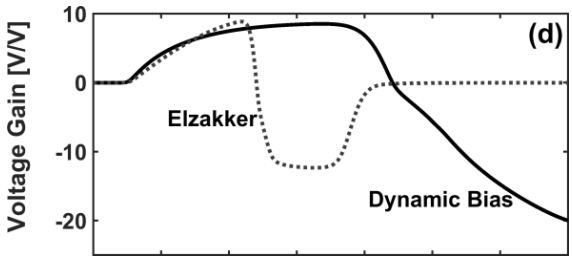


Figure 19 Voltage Gain Comparison.

In order to achieve the goal of reducing the power dissipation of the circuit, some data indicators are modeled below. The formula of the model is as follows.

$$A_V(T_{\mathrm{INT}}) = \frac{C_{\mathrm{TAIL}}}{2n \cdot C_P} \frac{V_s(T_{\mathrm{INT}})}{\frac{kT}{q}} \tag{6}$$

$$\Delta V_{\mathrm{Di,CM}}(T_{\mathrm{INT}}) = \frac{C_{\mathrm{TAIL}}}{2 \cdot C_P} V_s(T_{\mathrm{INT}}) \tag{7}$$

It can be seen that the source voltage is a time-varying variable, and the voltage gain of the dynamic bias preamplifier is only related to C_P and C_{TAIL}, and C_P is not related to other design parameters as an independent parameter [9]. When the gain cannot meet the design requirement, the value of C_P should be adjusted first to make it attain the gain requirement.

$$E\left[v_{\mathrm{n,SI,\,in}}^2\left(T_{\mathrm{INT}}\right)\right]=\frac{4kT\Upsilon}{C_P\cdot\Delta V_{\mathrm{Di,CM}}(T_{\mathrm{INT}})\cdot\left(\frac{g_m}{I_{\mathrm{CM}}}\right)_{\mathrm{SI},T_{\mathrm{INT}}}} \tag{8}$$

$$E\left[v_{\mathrm{n,WI,in}}^2(T_{\mathrm{INT}})\right]=\frac{2nkT}{C_P\cdot\Delta V_{\mathrm{Di,CM}}(T_{\mathrm{INT}})\cdot\left(\frac{g_m}{I_{\mathrm{CM}}}\right)_{WI,T_{\mathrm{INT}}}} \tag{9}$$

Formulas (8) and (9) are the noise analysis and calculation formulas when the circuit works in the strong inversion region and the weak inversion region, respectively. In order to obtain a smaller input noise, the value of C_P should be as large as possible, and g_m should be as small as possible.

It can be seen that, the circuit operates in the strong inversion region when the value of V_{GS}-V_T is greater than 0, and when V_{GS}-V_T is less than 0, the circuit operates in the weak inversion region [10].

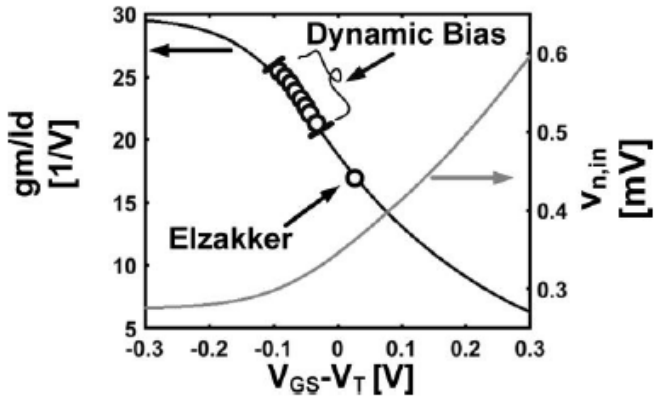


Figure 20. Relationship between gm/Id and input reference noise voltage to VGS-VT.

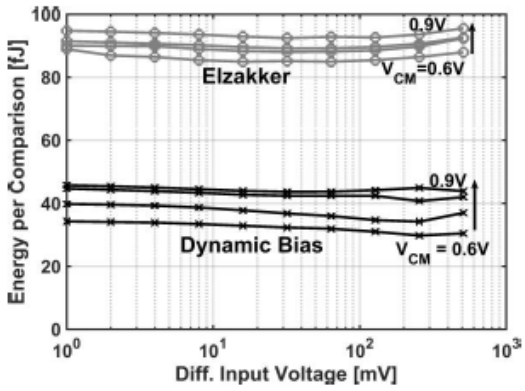
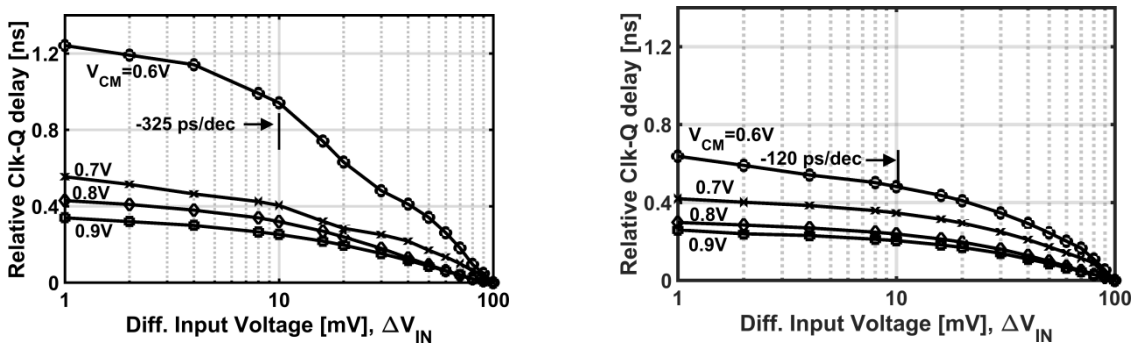


Figure 21. Energy dissipation of dynamic bias and Elzakker's comparator

From Figure 20 we can see that the gm/Id of the dynamic bias comparator changes from $20V^{-1}$ to approximately $25V^{-1}$ during the integration time, when the dynamic bias preamp's V_{CM} = 0.6V， the range of V_{GS}–V_T is approximately -25 to -100 mV. Therefore, the dynamic bias comparator works in the weak inversion region.

There are also some design parameters and the relationship between design indicators that cannot be reflected by mathematical modeling, and they are presented in the article by simulation.

When the common mode voltage is between 0.6-0.9, the larger the common mode input is the greater energy consumed. In Elzakker's comparator, under the same common-mode voltage, the power dissipation is much greater than the dynamic bias. At a common-mode voltage of 0.7, the power dissipation of the circuit is approximately 15% higher than that at a common-mode voltage of 0.6.



(a) (b)

Figure 22 Relative CLK-Q delay for the (a) dynamic bias comparator and (b) Elzakker's comparator.

It can be obtained that under the same common mode input, the delay of the dynamic bias comparator is slightly larger than that of Elzakker's comparator. When the common-mode input of the dynamic bias amplifier changes from 0.6 to 0.7, the delay decreases by more than 50%, and the change is the most severe at this time. In order to control the delay and leave some variation range, the common mode input should be between 0.7-0.8V. At this stage, the power dissipation has increased by only 15%, but the delay has dropped by more than 50%.

We will analyze it in combination with Figure 20. Because the comparator works in the weak inversion region, when the common mode value is 0.6, although its input referred noise is better and the power dissipation is lower, it is precisely because the current in this region is too small, it causes the delay to be too large, so it is inappropriate to choose 0.6.

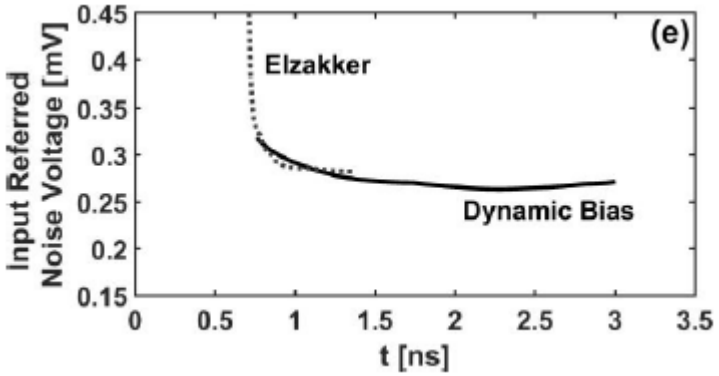


Figure 23. Input Referred Noise Comparison

Many works have been done to improve the power dissipation, and at the same time the input noise has also improved (showed in Figure 23), although the delay part has not been optimized enough.

3. Conclusions

The improvement point of the pre-amplifier improved comparator is the use of PMOS latches and PMOS preamplifiers, expect a small cross-coupling circuit, a special clock mode is used to adjust the gain of the preamplifier. The clock mode provides sufficient preamplifier gain to achieve the goal of increasing comparator speed and greatly reducing power dissipation. The switch separated latch comparator is discussed in second part which added switch in latch section. The use of switches changes the operating state under different conditions, thereby enhancing the entire transconductance of the latch, so that the delay and energy dissipation are significantly reduced.

Another innovative dynamic bias comparator presented in this paper has the following characteristics. For a given capacitive load, the noise of the preamplifier can get maximization by increasing gm/Id. The performance of the dynamic bias comparator can be optimized by adjusting the ratio of the tail capacitance to the load capacitance at a given common-mode voltage. Therefore, the method of adding a resistor to the tail current source part can solve these problems from the root.

Although the design only optimizes power dissipation and noise, there is no obvious optimization in delay, so this is the focus of work that needs to be further improved in the future.

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