The Application of Two Stage Amplifier Based on CMOS in Amplification of Electrocardiogram

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Abstract. With the purpose of detecting heart diseases, electrocardiogram monitor is created, which records the micro electrical activity of the heart muscle. In the paper, a two stage amplifier is design to amplify the signal in a observable level. It is based on CMOS of TSMC 0.18 μm technology with 1.8 V supply voltage. The total gain Direct Current (DC) gain is around 87 dB and -3dB bandwidth is about 3000Hz. After adding a 0.1 pF compensation capacitor, the phase margin obtained is 91.57°. Also, the total current consumption of the amplifier is less than 6 μm, which is 5.21 μm. Please note that the simulation and analysis is operated on Coolspice Software. This two stage amplifier could be an alternative choice applied in the ECG monitor in order to increase the performance of the wave interpretation.

Keywords: CMOS, electrocardiogram monitor, two stage amplifier, Coolspice Software.

1. Introduction

Heart diseases are well-known for the major damage they cause to human body. They can also become fatal to people's health in extreme cases. One way to check whether the heart is in a healthy condition is to use the "ECG" monitor. "ECG" is the abbreviation of electrocardiogram. This machine detects micro electrical activity of the heart by placing electrodes on the skin. Even the small voltage changes caused by the muscle around the heart can be discerned by these electrodes. The result presents in two forms. Doctors use a moving paper to record heart activities and that paper is usually for patients to keep. Another way is to present the moving line of the heart activity on digital screen, which is often utilized in intensive care unit with the purpose of real time monitoring [1].

As mentioned above, the electrical signal detected from heart is extremely weak. Therefore, it is necessary to create an amplifier which provides high voltage gain. In this essay, an idea of producing a two stage amplifier based on CMOS is proposed. Generally, there are two parts in the amplifier which is a differential amplifier and a common source amplifier both to generate high gain. Only the 0.18 μm technology CMOS is applied. The only way of achieving desired result is to scale the aspect ratio of MOSFET. The details of specification of the design would be discussed later in the section three.

In this paper, the research is beneficial to increase the performance of the amplifier during the process of reading ECG signals, which gives further improvement on the quality of imaging ECG graph. This suggests appropriate method to specified details of ECG interpretation.

2. Working Principle of Electrocardiogram

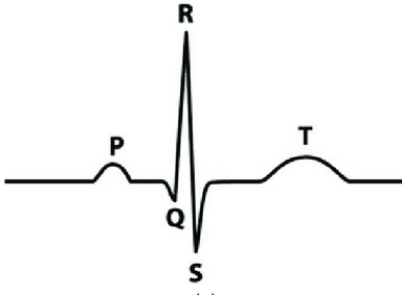


Figure 1 General ECG Interpretation [2]

Moving to the next section, the first step is to present a briefly introduction to the ECG waves. Generally, the waves would be separated into three phases: P-wave, QRS complex and T-wave, as illustrated in Figure 1. P-wave is the start phase of ECG wave, which corresponds to atrial depolarization. It indicates that whether the impulse conduction from atria to the ventricle is normal. Between the P-wave and QRS complex, the flat line is named PR segment, which corresponds to atrioventricular. It also known as the reference line of ECG wave. The amplitude of QRS complex is much greater than P-wave. Since the muscle of left right ventricles is much stronger than atria. It records the signal that causes atria and ventricles contract and then pump blood to the body. Typically, the narrow QRS complex stands that the ventricles are depolarizes quickly, which is patients desire to see. The ventricles relax or called rapid ventricle repolarization is the reason to cause T-wave. Observed from graph, the T-wave is symmetric. However, it is not the fact in most cases. The downwards slope drops slightly more than the upward slope [3].

After the introduction of ECG interpretation, how to detect potential difference is concerned. With the purpose of simple application, there are usually four electrodes placement (left arm, left leg, right arm, right leg) in three leads (left right legs connected, left arm and right leg connected, right arm and right leg connected) [4]. Note that electrodes are the conductive pads attached to the body surface [5]. Although the ECG interpretation is different in each lead, which is said that the peak value of the wave in three phases is not the same. The total tendency is quite similar [6].

In ECG monitor, one common application amplifier is the biopotential amplifier which has three stages: patient protection stage, instrumentation amplifier stage and high pass filter stage [4]. As its name, the first stage is to protect the patients. For example, the short circuit of the device would generate large current toward patient, which would be harmful to the safety. Therefore, the protection is achieved by adding diodes. In ideal circumstances, when forward bias current is applied, diode can be considered as normal wire. When reversed bias is applied, it acts as open-circuit, and any current cannot pass through. In real world, it would have some current leakage but would not exceed the safe value when reversed bias happens. These would protect both the patient and the device. The instrumentation amplifier is what the author desires to prove the performance with the two stage amplifier, which will have a detailed implementation later this section. The instrumentation amplifier utilizes three operational amplifiers. The first two amplifiers are to increase the value and the third one is to differentiate the input signals. The third stage usually applies RC filter to filter the low frequency such as movement and respiratory variation. Here is the example of how the filter affects the ECG interpretation which is presented below in Figure 2.

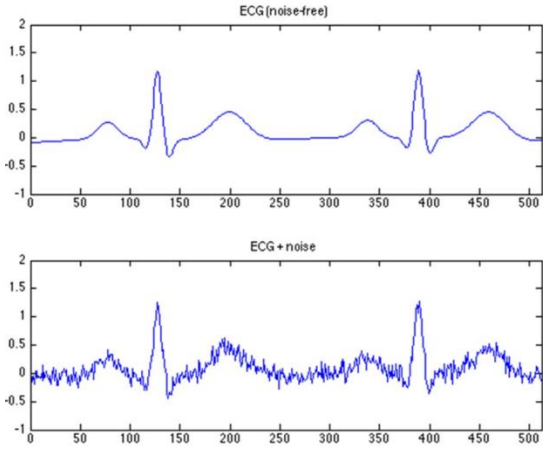


Figure 2 How the Filter Affect the ECG Wave [7]

3. The Design of Two Stage Amplifier Applied in Amplification Process

Since the last section discusses about the general process of electrocardiogram, this section would focus on explicit process of how to design a two stage amplifier to replace instrumentation amplifier. Firstly, it is about what is provided and required. For example, the performance that the amplifier is

required to achieve. Moreover, which components and supply are provided is concerned as well. In the second segment, the amplifier would be separated into three parts. Each part will have a clear explanation of how it works and what it is utilized in the two stage amplifier. After the schematic presented, the essay concentrates on result and discussion.

3.1. Design Preparation and Requirement

Turning to the first segment, through this design of the amplifier, only the 0.18μm technology which is named as C018 CMOS is applied. Based on the technology, the experiment would choose the standard 1.8 V as the voltage applied to the drain of the transistors (Vdd supply) [8]. The bias current is certain to 2μA and would be transformed through current mirror. In the stage of differential amplifier, the large signal is 0.9V. The reason behind 0.5V alternating current signal select is that the differential voltage would be fix to 1 volt. According to equation (1), the voltage gain is equal to the output voltage when input voltage is 1 volt. Since the dB is in logarithmic calculation (2), the input voltage in dB is 0 when it is 1 volt. The output voltage in dB is the same value as the gain in dB. Therefore, observed from the graph would be much easier. Additionally, a compensation capacitor would be added to adjust phase margin.

$$Voltage\ Gain = \frac{V_{out}}{V_{in}} \tag{1}$$

$$Voltage\ Gain\ in\ dB = 20log_{10}(Voltage\ Gain) \tag{2}$$

With the purpose of clear view, the design specifications are listed in the below table

Table 1. Design prepared

COMPONENT	VALUE/SIZE
2×C018 NMOS ---- N3, N4	W: 20 μm, L:1 μm
C018 NMOS ---- N5	W: 10 μm, L:1 μm
2×C018 NMOS ---- N1, N2	W: 180 μm, L:5 μm
2×C018 PMOS ---- P1, P2	W: 35 μm, L:6 μm
C018 PMOS ---- P3	W: 40 μm, L:5.9 μm
Vdd supply	1.8 V
2×Bias current	2 μA
Vac	0.5 A
Vdc	0.9 V

Table 2. Deaign specification

PARAMETER	VALUE
DC gain	>80 dB (10000V/V)
-3dB bandwidth	AT 3 KHz
Phase margin	>40 degrees
Total current consumption	<6 μA
DC gain	>80 dB (10000 V/V)

3.2. Circuit Design

Turning to the process of circuit design, the two stage amplifier is constructed by three parts: differential amplifier, common source amplifier and current mirror. The two amplifiers play an important role in creating high voltage gain. The current mirror is to provide drain current copied

from bias current. The diagram of amplifier is presented below. Please note that the compensation capacitor is added shown in Figure 3.

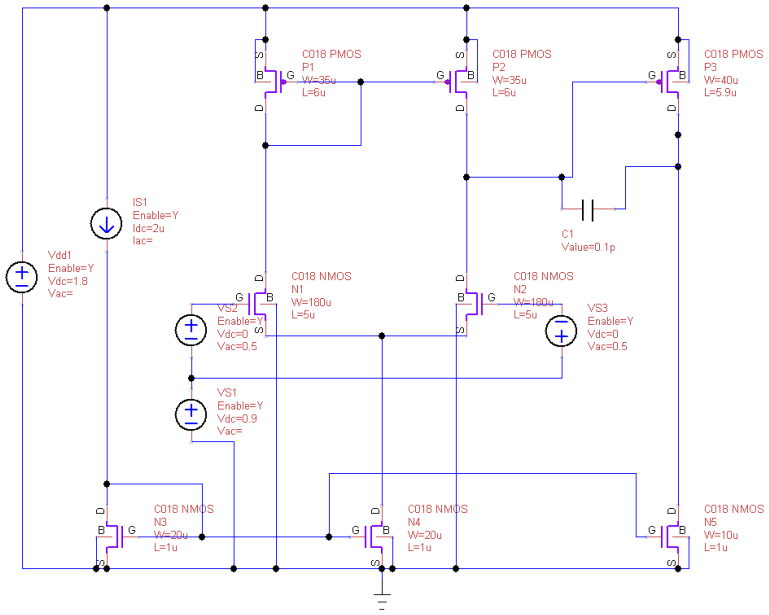


Figure 3 The Diagram of Two Stage Amplifier

3.2.1 Differential Amplifier

As shown in Figure 3, transistors N1, N2, P1, P2 consist of differential amplifier, which is also name as operational transconductance amplifier in detailed specification. The transistors N1 and N2 take the function of receiving signals and differentiating them. The way of differentiating is to set the positive and negative terminal of voltage source connected to N1 and N2 respectively. Then P1 and P2 are current mirror to carry the drain current to transistor P2, which become the drain current of P2. Since the drain current also exist in the transistor. The node current (output current) between two transistors is the result after subtracting from two drain current. Effectively, the resistance of transistor P2 is parallel to the resistance of N2. Hence, the difference current of transistor N1 and N2 is equal to the output current. And mathematically, the voltage gain could be calculated as follows:

$$Gain_v = g_m(r_{N2} \parallel r_{P2}) \tag{3}$$

Where the gm is the transconductance of the amplifier.

3.2.2 Common Source Amplifier

The PMOS common-source amplifier here replace the resistor with NMOS current mirror in the implementation. The bias current would be copied by the current mirror and then provide to the amplifier. The input voltage of the amplifier would be provided from the output voltage of operational transconductance amplifier. In the small signal analysis, since the DC voltage becomes AC ground, the resistance of P3 is parallel to the resistance of N5. Therefore, the voltage gain could be calculated as follows. And the output resistance can be calculated as well. To sum up, the common source amplifier can generate moderate high gain and high output resistance determined by equation (4) and (5).

$$Gain_v = g_m(r_{N5} \parallel r_{P3}) \tag{4}$$

$$R_o = (r_{N5} \parallel r_{P3}) \tag{5}$$

3.2.3 Compensation Capacitor

There is a capacitor placed between the output of differential amplifier and the output of common source amplifier named compensation capacitor. Generally, when gain of two stage amplifier is equal to the gain of 0 dB (1 V/V) – the unity gain frequency, the subtraction between corresponding phase

and 180 degrees would be less than 45 degrees, which is the phase margin [9]. The figure will be shown later in the result and discussion section. As a result, the system cannot satisfy the stability criterion [10]. Therefore, a capacitor is needed to compensate the phase margin, which enables the system to achieve stable.

3.3. Results and discussions

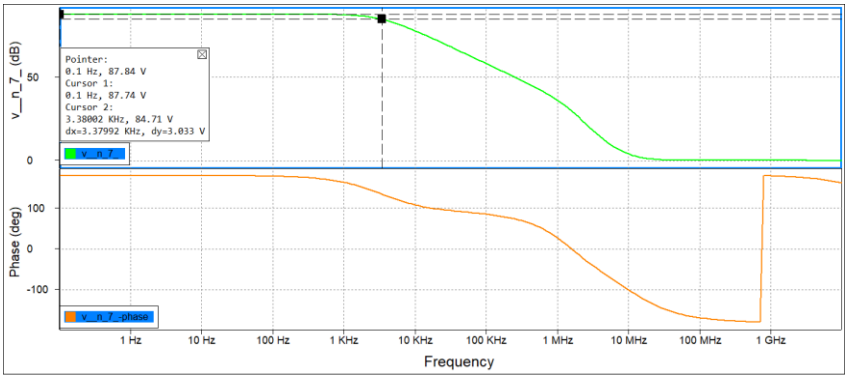


Figure 4 Frequency Response of the Amplifier

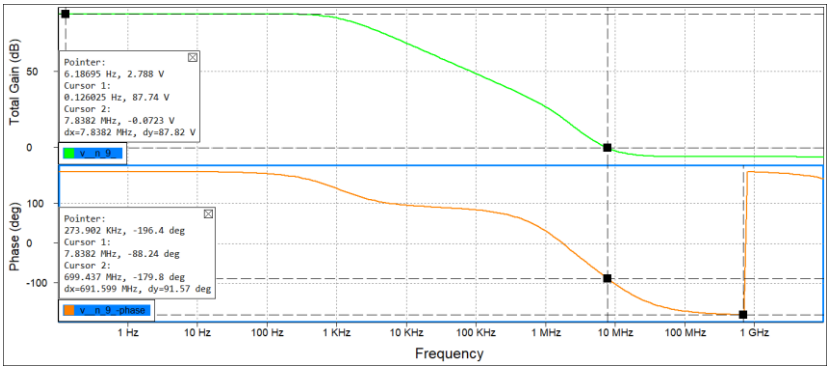


Figure 5 Compensation Capacitor Added

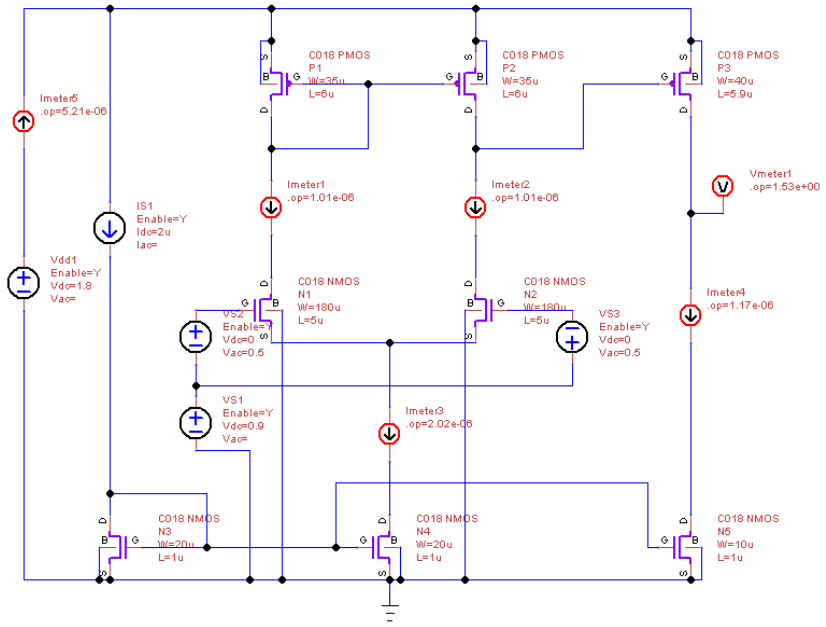


Figure 6 Total Current Consumption

All MOSFETs are working in saturation region to ensure the best performance condition. Before varying the frequency, the total current consumption is 5.21 μm illustrated in Figure 6, which follows the standard. When the frequency ranging from 0.1Hz to 1GHz, the result is illustrated as above in

Figure 4. The –3dB bandwidth is approximate 3.4 kHz, which is around the 3000 Hz requirement. The open loop gain obtained is 87.74dB. In feedback systems, the precision of operational amplifier is ascertained by open loop gain, which the reason it is extremely crucial. Generally, with the gain increment, the precision of the feedback system increases. Furthermore, the immense value of gain also benefits the observation of ECG signal to be interpreted on screen. After adding the compensation capacitor in the circuit, it is obvious that in Figure 5 the bandwidth decreases. And the phase margin measures as the value of 91.57 °, which is over the 40 ° requirement. It also determines that the stability of the system is great. Since the stability increases as the margin value growth in positive region [11].

4. Conclusion

In the paper, I briefly explained basic knowledge of ECG and a well-performed two stage amplifier is created. All transistors in the circuit are working in the saturation region to set the normal requirement. The total current consumption is 5.21 μm. In the AC simulation from the range of 1Hz to 10MHz, the total gain is 87.74 dB which reaches the standard. And the –3dB bandwidth obtained is around 3kHz. After adding a compensation capacitor to the circuit, the stability of the system is enhanced. The phase margin obtained is over 40 degree which is 91.57 degrees in the design. Hence, the two stage amplifier could meet the standard to replace the instrumentation amplifier, which provides an alternative application in the ECG monitor.

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