Review of Four Improving Designs of Dynamic Latch Comparator

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Abstract. In this paper, four disparate designs of dynamic latch comparators are discussed consecutively. By improving the design of the pre-amplifier stage, the double tail comparator provides a good power-speed trade-off. Further, Differential pair amplifiers are implemented in the second design, which has better comparison speed and energy dissipation. Next, a bulk-driven structure is employed on the comparator design to improve the comparison speed. Finally, a dynamic comparator utilizes a floating reservoir capacitor and a positive feedback bulk structure is introduced to achieve higher energy efficiency. The overall performance of these comparators is evaluated in this paper.

Keywords: Dynamic Latch Comparator, Pre-amplifier stage, Double tail comparator, Differential pair amplifier, Dynamic comparator.

1. Introduction

The development of low-power and high-speed analog-to-digital converters (ADCs) is one of the key components for implementing various portable electronic devices. Comparator is vital to the efficiency of flash ADCs among other parts of the structure since it is directly related to the performance and accuracy of the device. To enhance the performance of such a device, the comparator is designed to be power-efficient, low-noise, and high-speed. In general, a faster and more accurate comparator is demanded to lower the overall energy consumption and increase the speed of a circuit [1]. Therefore, four innovative designs are compared in this article.

In 2019, Mehrdad Amirkhan Dehkordi and his team proposed the double-tail structure of the dynamic latch comparator. By firstly introducing the double-stage design that contains the pre-amplifier stage and the latch stage, the double-tail design achieved a lower energy consumption [2]. However, though the circuit uses a time-domain bulk tuned offset cancellation technique to decrease the offset voltage that reduces energy consumption, the circuit is also slower than similar designs because of that [3-4].

To achieve higher speed, Zhengbo Huang and his team proposed some enhancement that incorporates a bulk-driven structure in the comparator design. As a result of coupling the input signal to bulk nodes in comparison phrases to increase the transconductance, the new structure increased the speed of the comparator and lower the power consumption at the same time [5]. Another structure proposed by J´erome K. Folla and his team signifies a similar direction of improvement in comparison speed. The idea is to avoid parallel oscillation and short circuit power dissipation in the latch stage with a differential pair amplifier which has the enhancement- NMOS, and thus reduce the parasitic capacitance and enhance the trans-conductance [6].

Lastly, Bruno Canal and his team proposed the new bulk-effect-based structure on a floating inverter amplifier. Canal applied a charge sharing scheme to improve the speed of the circuit and a dynamic bias is proposed for the pre-amplifier, which reduces the power consumption. Following the idea of dynamic biasing, a floating inverter amplifier (FIA) is used to operate with a low-voltage and low-noise environment. The paper is organized as follows. Section II presents the analysis of the four reviewed designs of dynamic latch comparator related to its time-delay, kick-back noises, operation in different temperatures, and energy dissipation [7]. Section III will show the comparative result of the four comparator structures and analyze the advantages and disadvantages of each of them. Section IV is a summary of the article.

2. The Double Tail Comparator

Mehrdad Amirkhan Dehkordi and his team have proposed a two-staged dynamic comparator, which reduces the power-delay product parameter and energy consumption. On the basis of the power-speed trade-off, the comparator can be used against low power consumption. The fundamental idea of the new design is to separate the comparator working stages into two parts [8]. The first part is to amplify the signal to make it diagnosable, and the second part is to detect the amplified signals and to compare the value of those two signals when they are differing in relative large value.

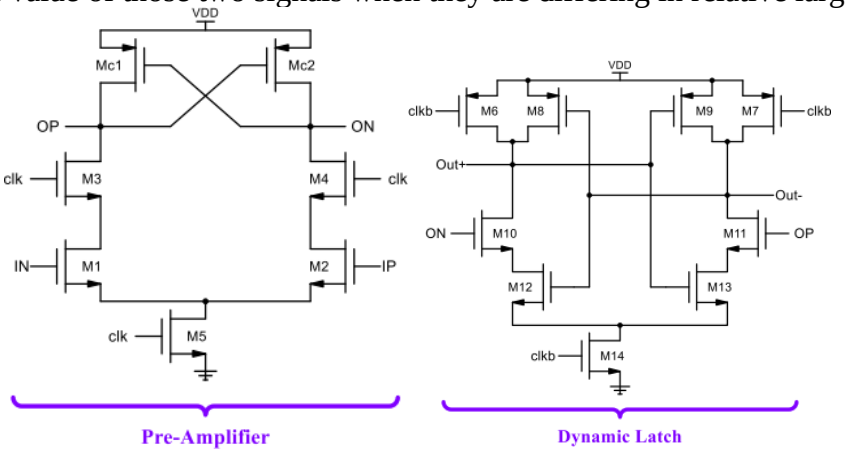


Figure 1. The proposed two stage dynamic comparator structure (Pre-Amplifier). [1]

As Fig 1 shows, compared with traditional comparators, the new design separates the circuit into two stages, the pre-amplifier stage and the Latch stage, to isolate the input and output nodes. The two M11 and M12 transistors connect the two sections and transmit voltage FP and FN to the inverters. To calculate the delay of the two-stage dynamic comparator, the group has shown the calculation of function of delay is:

$$T_{Comp} = T_{P\ re-amp} + T_{Latch} \tag{1}$$

$$T_{P\,re-amp} = \frac{C_{OP}+C_{ON}}{I_{M5}} \times V_{thM10,\ M11} \tag{2}$$

$$T_{Latch} = T_0 + \left(\tau \times \ln\left(\frac{0.5(VDD-GND)}{V_{dm}}\right) \right) \tag{3}$$

2.1. Result

The transient simulation results of the proposed dynamic comparator circuit for Vdm=5mv, Vcm= 0.7 V, and VDD =1V, with the operating frequency =500 MHz. It shows that the time when the voltage gap reaches ½ Vdd is about 0.03ns which is generally better than the traditional design, as shown in Figure 2 and Figure 3.

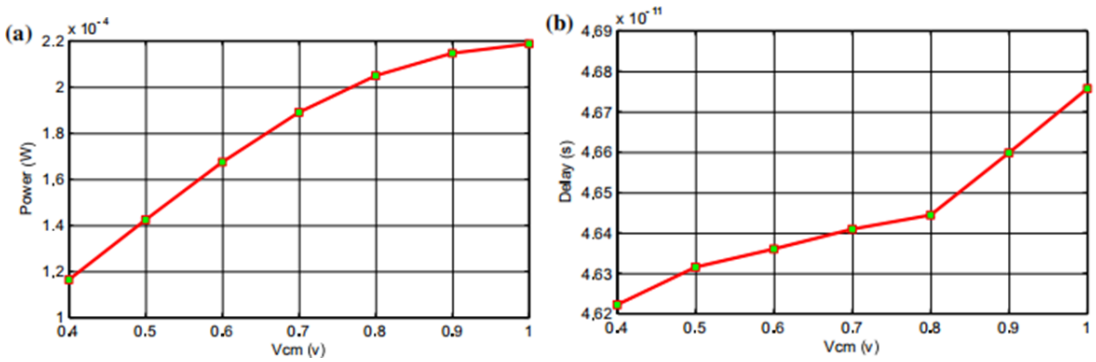


Figure 2. The power variation due to the input common mode voltage [1], and the delay variation due to the input common mode voltage

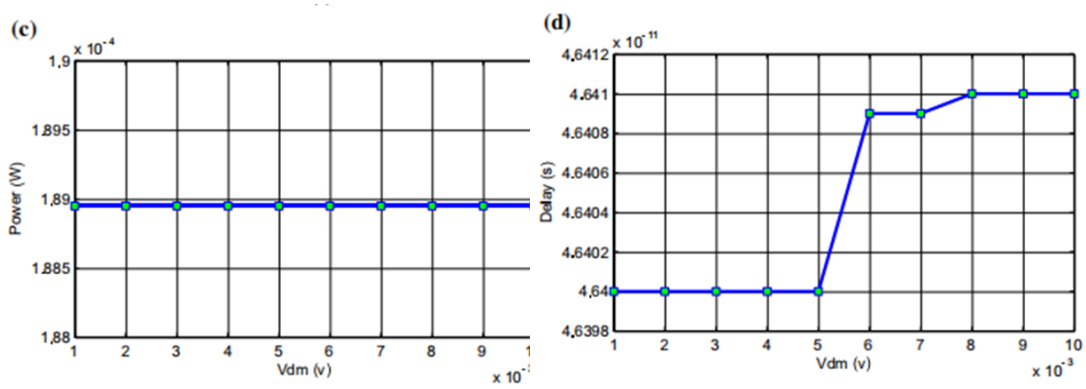


Figure 3. The power variation due to the differential input voltage [1], and the delay variation due to the differential input voltage

Also, by increasing the common-mode input voltage, the power consumption of the circuit will increase dramatically. Meanwhile, as shown on the graph, the power consumption has a positive relation with Vcm and no effect on Vdm, since Vcm is positive to the circuit delay, it can conclude that the power consumption is positively related to the circuit delay [9]. In the concept of low power and low delay in the circuit, it will be reasonable to select 0.5 to 0.6 as the applicable Vcm of the comparator, as shown in Table 1.

Table 1. Performance of proposed comparator in different temperature

Temp ($^{\circ}C$)	-10	25	40	60
Power (μW)	197.47	188.9	179.06	171.69
Delay (ps)	38.7	46.4	50.4	55.8
PDP (fJ)	7.64	8.76	9.02	9.58

When the design was engaged in different temperatures, the power consumption is generally lowered when temperature increases and the delay is nearly positive to the increased temperature, and the slope of which is .2ps/degree of celsius if we apply 1D line fit to the graph. Also, the PDP is more unstable when the temperature is above room temperature. Hence, the best conduction temperature of the design is around or below room temperature [10].

2.2. Pre-amplifier Stage Enhanced Comparator

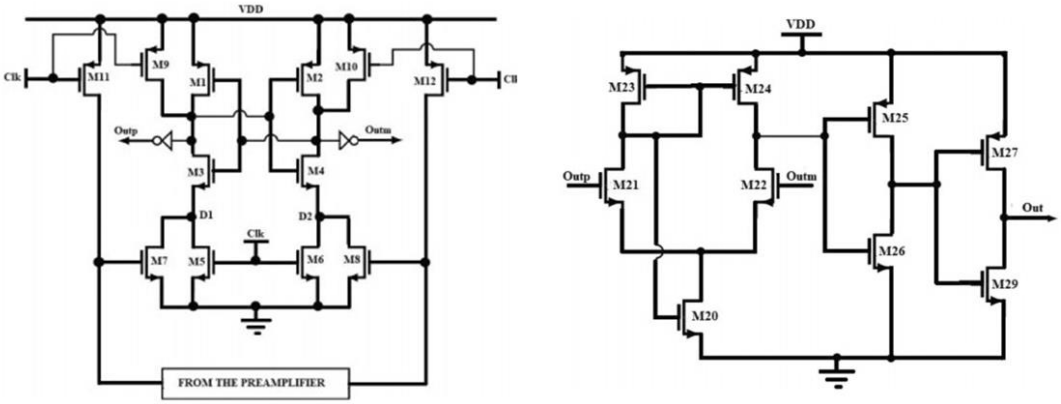


Figure 4. block diagram of the proposed dynamic comparator [2], and the proposed dynamic comparator structure

Though the double-tail design outweighs the traditional comparator design, the J´erˆome K. Folla, Laboratory of Energy with his group introduced a new design called dynamic latch comparator with a higher gain and lower offset compared to double tail design, as shown in Figure 4. By applying a differential pair amplifier that contains enhanced load NMOS, the dynamic latch design will have

lower power consumption and higher comparison speed. To calculate the delay of the proposed dynamic comparator, the group has shown the calculation of function of power dissipation is:

$$P_{total} = \frac{2C_L V_{DD}(V_{DD} - V_{TH\,N})}{T_{dk}} \tag{4}$$

and the time delay can be calculated as:

$$t_{delay} = t_{dis} + t_{latch} \tag{5}$$

$$t_{delay} = \frac{t_0}{(1+\frac{g_{mN}}{g_{mP}})^2} + \frac{t_{latch}}{1+\frac{g_{m11,12}}{g_{meff}}} + \frac{2C_{out}}{g_{meff}+g_{m11,12}} \ln\left(\frac{1+\frac{g_{mN}}{g_{mP}}}{g_{m16,17}(g_{m5,6}+g_{m7,8})}\right) \tag{6}$$

Now let's look at the simulation process and the result: As the data are shown below, though the general trend of the proposed and the conventional design is the same that the kick-back noise is decreased with higher Vin, the proposed kick-back noise is lower than conventional for every Vin. Hence the general kickback noise is lower for the proposed design [11]. Also, when the input voltage increases, the time delay dropped significantly as to the higher VDD; thus, to lower the time lay of the proposed circuit as well as the kick back noise, the input voltage should be controlled at a range between 0.8-1.1v, as shown in Figure 5 and Figure 6.

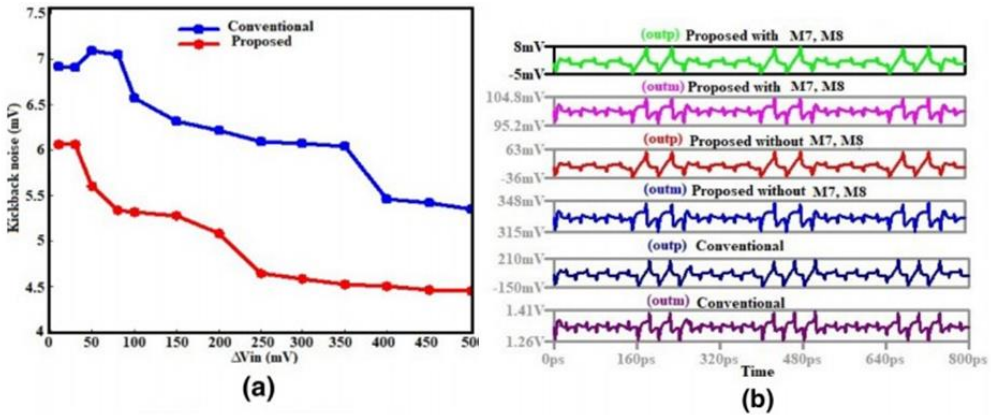


Figure 5. The kick back noise versus differential input voltage, and δVin =20mV[2]

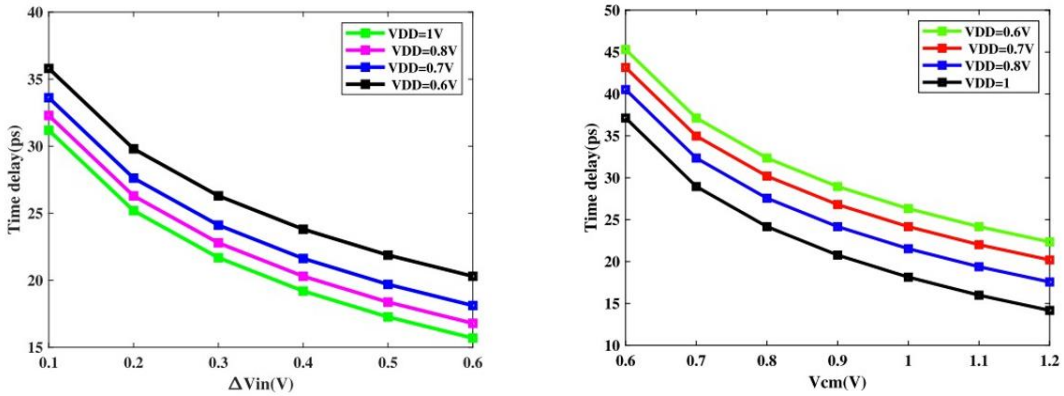


Figure 6. The delay versus differential input voltage, and delay versus input common mode voltage [2]

As Figure 7 shows, the power consumption is lowest in simulation when the Vcm is between 0.7 and 0.8 volt, and it shows a higher performance when δVin is between 0.5 to 0.6 volt Thus in consideration of power consumption and time delay trade-off, the input common mode voltage of the circuit is suggested to work between 0.6-0.7 voltage to gain low power consumption as well as relative lower time delay. Lastly, the group test the power consumption of the proposed design in different

temperature, and it is clear that circuit has better performance at lower temperature. Thus, since the design aim to achieve ultra-low power dissipation, it is legible to let the comparator working at lower temperature.

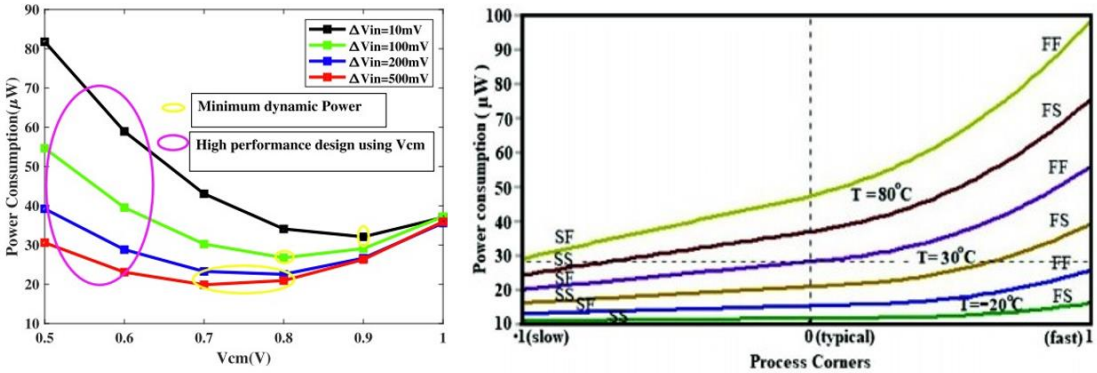


Figure 7. Power consumption versus input common mode voltage, and the power consumption versus working temperature [2]

3. The Bulk-driven Comparator

Zhengbo Huang and his team proposed some enhancement that incorporates a bulk-driven structure in the comparator design. On the basis of the latch structure, the Zhengbo's group designed a 65nm CMOS low-Voltage Comparator. In the new proposed structure, an NMOS- input pre-amplifier is designed to offset kick-back noise before the latch. In addition, the bulk driven technique is implemented along with the cross-coupled NMOS transistors in separated N-wells.

In the result analyze and simulation, it is clear that the proposed structure gas better control of delay of latch compared with the traditional design since the probability graph shown that the mean time of delay and the median time of delay is lower than conventional design, and the standard deviation is also of smaller value compared with traditional design, as shown in Figure 8, Figure 9 and Figure 10.

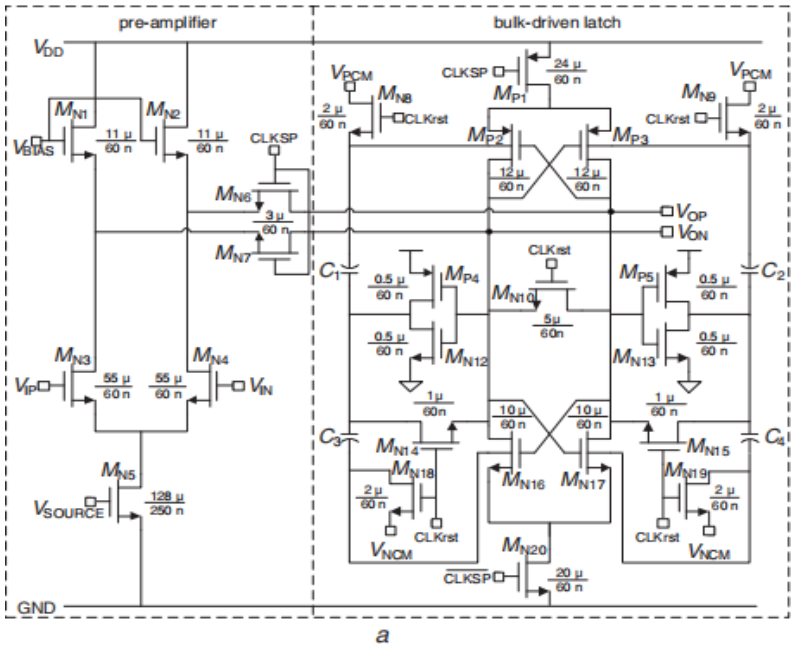


Figure 8. Schematic diagram of the proposed design [3]

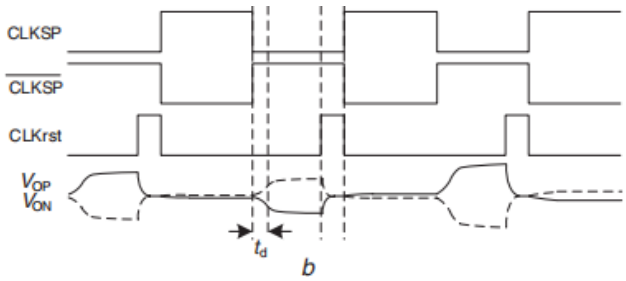


Figure 9. Time diagram of the proposed design [3]

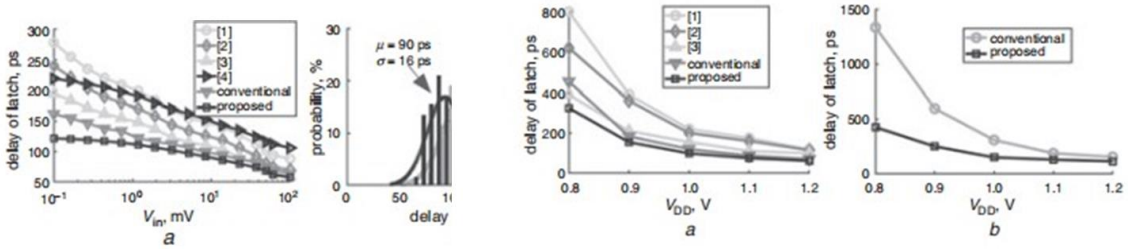


Figure 10. Compare the delay of latch with conventional design, and the delay of latch versus V_{DD} (a for 50mV input, b for 0.1mv input) [3]

Further, by analysis of relationship between V_{DD} with delay of latch, the group found that the delay of latch become stable after V_{DD} reach 1.0v and higher volt. So, to lower the delay of latch of the comparator circuit, the V_{DD} should be controlled above 1 v, as shown in Figure 11.

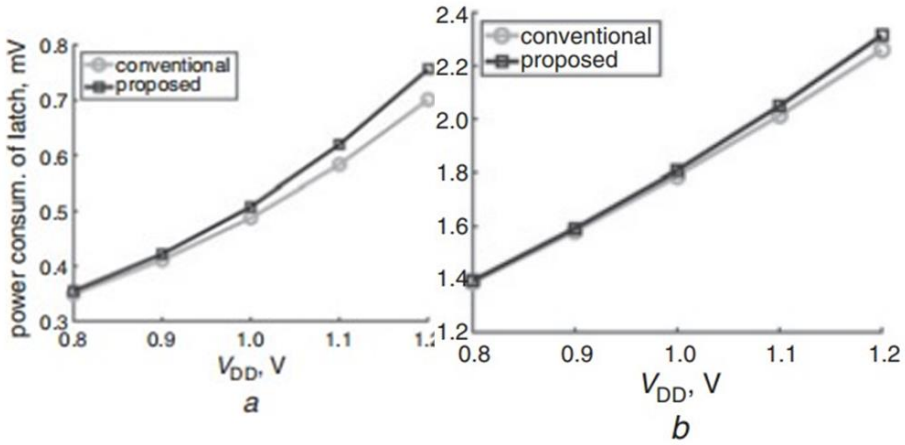


Figure 11. Core latch power consumption versus V_{DD}, and Whole comparator power consumption versus V_{DD} [3]

Lastly, by analyzing power consumption with V_{DD}, the proposed structure shows less control on power dissipation when V_{DD} is higher than 1.0V; thus, to control a reasonable power consumption in the circuit, the ideal V_{DD} should be between 1.0-1.1 V to reach a balance of power consumption and delay of latch.

4. Floating Inverter Amplifter Comparator

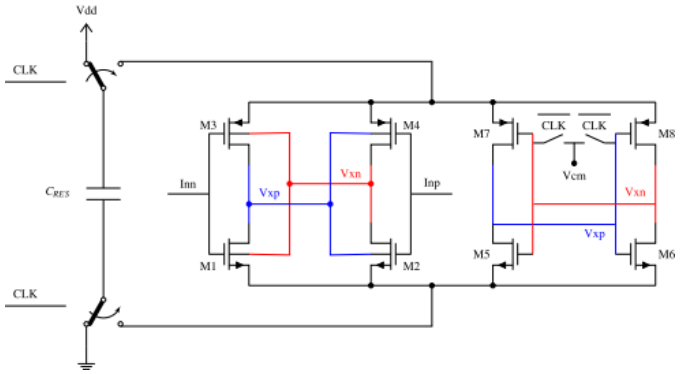


Figure 12. The proposed structure [4]

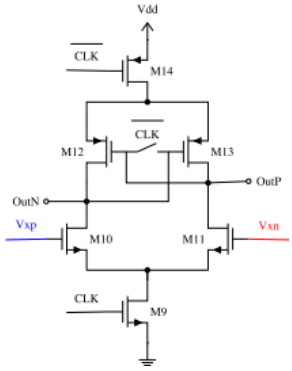


Figure 13. The proposed structure [4]

As shown in Figure 12 and Figure 13, preamplifier for Positive Feedback Bulk FIA (PFB-FIA) It is proposed here to take advantage of the low noise characteristics and the power supply strategy. Floating reservoir capacitors provide an isolated power domain that makes the pre-amplifier less Global process variability, as shown in Figure 14. The tansconductance in saturated operation is approximated through:

$$g_m = \frac{2s}{n\phi_i} \cdot \sqrt{1+i_f} \tag{7}$$

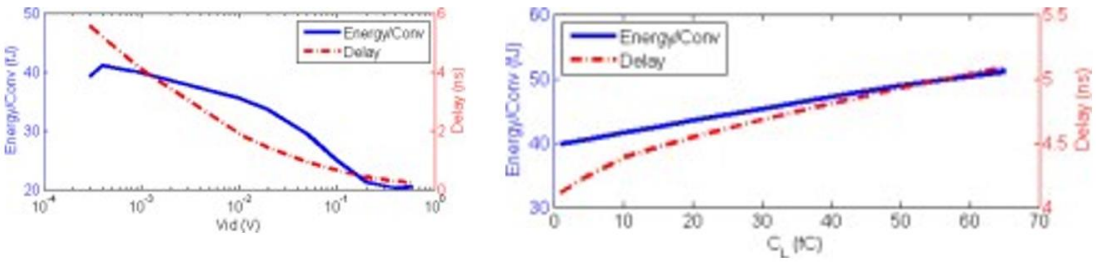


Figure 14. Energy per conversion and delay as function of differential input voltage, and energy variation versus C_L [2]

In the simulation, it is clear to observe a negative relation between the energy per conversion and delay as function of differential input voltage. So it is reasonable to select Vid between 10−1 and 100. Also, the delay- temperature revels the higher working temperature is better for the proposed design, and in consideration of power consumption, it is reasonable to let it work at higher temperature since Lower temperatures worsen the influence of the corner variability on delay.

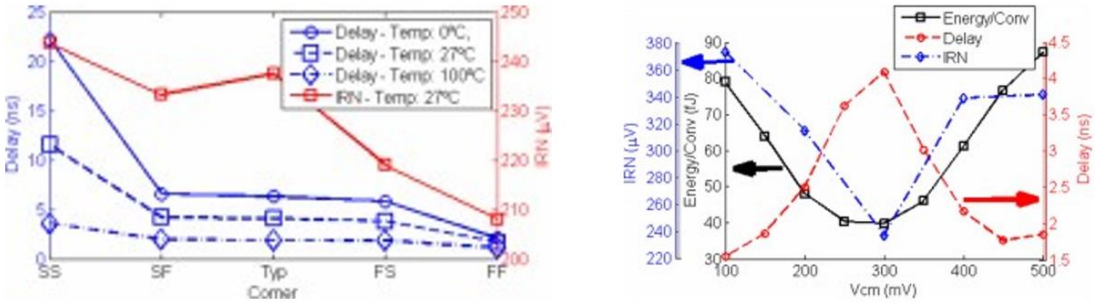


Figure 15. Dealey in different temperature, and input referred noise, energy per conversion and delay as function of common mode input voltage [2]

Also consider the power dissipation with relation to Vcm, Variations in the input- common voltage alter the input gain between PMOS and NMOS push-pull differential pairs, which results in a change in the VX common voltage. In consideration of working Vcm, the delay, the energy consumption, and the input referred noise coincide at range of Vcm of 200 mv to 250mv and 350mv to 375mv. Since the delay is lower when Vcm is higher, so it is considered reasonable to choose 350mv to 375mv as the proposed Vcm for the new design, as shown in Figure 15.

5. Conclusion

In conclusion, the Double Tail Comparator is relatively outdated, so its performance is worse than other newly designed comparator. The Pre-amplifier Stage Enhanced Comparator has the lowest power consumption, and the Bulk driven comparator has the lowest supply voltage. Lastly, the floating inverter Amplifier has the newest process and the lowest delay, as shown in Table 2.

Table 2. Peering comparation of four comparators

	The Double Tail	Pre-amplifier Stage Enhanced	The Bulk-driven	Floating Inverter
Process (nm)	90	65	65	28
Supply (V)	1	1	0.05	0.6
Power (mW)	0.188	0.067	0.75	
Delay (ps)	46.4	14.28	67	0.005

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