Real-Time Junction Temperature Estimation for Using Temperature-Sensitive Electrical Parameters

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Abstract. Silicon Carbide Metal-Oxide-Semiconductor Field-Effect Transistors (SiC MOSFETs) are core components in high-power systems like new energy vehicle powertrains and solar inverters, thanks to their high breakdown voltage, low on-state loss, and strong high-temperature tolerance. However, their junction temperature (T_J) rises sharply under high-power/frequency operations, and extreme T_J fluctuations cause solder cracking or wire bonding detachment, shortening service life and risking system failure. Accurate real-time T_J measurement is critical for reliability. Traditional methods have flaws: infrared thermometers lack real-time capability, and built-in sensors require device redesign. Temperature-Sensitive Electrical Parameters (TSEPs)—which use the device' s intrinsic electrical parameters (correlated with T_J)—offer a non-invasive solution without physical contact or design changes, becoming a key research focus. This paper first classifies common TSEPs (static: $R_{DS,ON}$, $V_{DS,ON}$; dynamic: $T_{D,OFF}$, V_{VTH}) and explains their temperature sensitivity and application scenarios. It then elaborates on three T_J prediction models: traditional mathematical models (polynomial fitting, thermal network fusion), data-driven models (BPNN, DNN), and multi-TSEP fusion models. A specialized experimental circuit for TSEP acquisition (using Kelvin source parasitic inductance and digital isolation) is also presented, enabling real-time measurement in one PWM cycle. Finally, the paper identifies practical challenges (parasitic interference, aging-induced accuracy loss, poor extreme-condition adaptability) and proposes solutions like Kelvin connections and adaptive calibration. Future directions include exploring stable TSEPs and integrating measurement circuits into miniaturized chips, supporting SiC MOSFET thermal management and reliability.

Keywords: SiC MOSFET; Junction Temperature Estimation; Temperature-Sensitive Electrical Parameters (TSEPs); Data-Driven Modeling.

1. Introduction

SIC MOSFETs are favored in various high-tech fields due to their capabilities of withstanding high voltages, operating at high frequencies, and tolerating high temperatures. For instance, they enhance the efficiency of electric vehicle engines and solar power inverters. Nevertheless, when operating under high power, their internal junction temperature often increases significantly. Excessively high T_J or rapid T_J fluctuations can lead to issues like solder cracking and wire bonding detachment, resulting in device failure. Thus, accurate T_J measurement is crucial for ensuring the reliable operation of SiC MOSFETs [1].

Traditional T_J measurement methods have notable limitations. Infrared thermometers cannot achieve real-time measurement, and built-in temperature sensors require modifications to the device design. TSEPs address these problems by utilizing the device's inherent electrical parameters (which vary with temperature) to estimate T_J without physical contact or device modification. This makes TSEPs a focus of current research [2,3,4]

Researchers have investigated two main categories of TSEPs: static and dynamic. Static TSEPs include on-state resistance ($R_{DS,\,ON}$) and on-state drain-source voltage ($V_{DS,\,ON}$). $R_{DS,\,ON}$ increases approximately linearly with T_J, with a sensitivity of up to 3-7 mΩ/°C. However, its value changes as the device ages. Dynamic TSEPs consist of switching delay times ($T_{D,\,ON}$/$T_{D,\,OFF}$) and voltage change rate (dV_{DS}/dt). $T_{D,\,OFF}$ (turn-off delay) lengthens as T_J rises, with a sensitivity of around 1.642 ns/°C, but it is affected by load current [1,5].

Early studies primarily used a single TSEP for modeling, which resulted in insufficient accuracy. Currently, researchers are combining multiple TSEPs or employing AI models (such as neural networks) to improve accuracy. They also incorporate methods to compensate for errors caused by device aging [2].

This paper first introduces the selection of TSEPs and the analysis of their characteristics. Then, it explains different models for T_J prediction using TSEPs. Next, it presents an experimental circuit for TSEP measurement and model verification. Finally, it discusses the challenges of applying these methods in practical products and proposes future research directions.

2. Characteristics of TSEPs for SiC MOSFETs

2.1. Static TSEPs

2.1.1 On-State Resistance ($R_{DS, ON}$)

$R_{DS, ON}$ refers to the resistance between the drain and source when the device is in the on-state. It comprises channel resistance and drift region resistance. As T_J increases, the mobility of charge carriers (inside the device) decreases, leading to an increase in $R_{DS, ON}$. For example, the $R_{DS, ON}$ of the ROHM BSM400D12P2G003 module changes by 3-7 mΩ for each 1°C increases in T_J, and the linear correlation between $R_{DS, ON}$ and T_J is strong ($R^2 > 0.99$). However, after 6337 power cycles (a test simulating long-term use), the accuracy of $R_{DS,ON,}$on declines, causing a T_J measurement error of 18°C. The advantage of $R_{DS, ON}$ is its ease of measurement can be calculated using $V_{DS, ON}$ and drain current (I_{DS}), making it easily integrable into small control chips [1].

2.1.2 On-State Drain-Source Voltage ($V_{DS, ON}$)

$V_{DS, ON}$ is equal to the product of I_{DS} and $R_{DS, ON}$. Since $R_{DS, ON}$ varies with T_J, VDS, ON also changes with T_J. However, $V_{DS, ON}$ is affected by I_{DS}, so simultaneous measurement of I_{DS} is necessary. For the SCT3060AL device, when I_{DS} is fixed, $V_{DS, ON}$ changes by 2-3 mV for each 1°C increases in T_J. The measurement error is less than 15% within the temperature range of 25-150°C. To reduce the impact of I_{DS}, researchers use third-order polynomials for data fitting [1,6].

2.1.3 Body Diode Forward Voltage ($V_{DS, DIODE}$)

2.2. Dynamic TSEPs

2.2.1 Switch Delay Time ($V_{D, ON}/V_{D, OFF}$)

$T_{D, OFF}$ is the time required for the device to turn off. As T_J increases, the threshold voltage (V_{TH}) of the device decreases, slowing down the discharge of the gate capacitor and prolonging $T_{D, OFF}$. At a bus voltage of 100 $V_{D, OFF}$) changes by 1.642 ns for each 1°C increases. When the current load increases from 5A to 30A, the measurement error rises to 5%. To address this, researchers combine $T_{D, OFF}$ with turn-off voltage overshoot (V_{PEAK}) to establish a linear model: $T_J = 6.695\text{Vpeak} + 1.642T_{D, OFF}$ 1944, which achieves high accuracy (R^2 = 97.69%). $T_{D, ON}$ (turn-on delay) decreases with increasing T_J but has low sensitivity, so it is rarely used independently.

2.2.2 Virtual Threshold Voltage (V_{VTH})

Devices with a Kelvin source (S') have a small parasitic inductance ($L_{S'S}$) between the Kelvin source and the power source. Using this inductance, researchers can extract four TSEPs: virtual turn-on threshold voltage ($V_{VTH, ON}$), virtual turn-on delay ($T_{VD, ON}$), virtual turn-off threshold voltage ($V_{VTH, OFF}$), and virtual turn-off delay ($T_{VD, OFF}$). These parameters reflect the variation of V_{TH} with T_J. $V_{VTH, ON}$ changes by -11.5 mV for each 1K increase in T_J, and $T_{VD, OFF}$ changes by 370 ps for each 1K increase. The key advantage is that no additional circuits are needed—all four parameters can be measured within a single switching cycle, enabling rapid measurement [7].

2.2.3 Voltage/Current Change Rate (dV_{DS}/dt, dI_{DS}/dt)

dV_{DS}/dt represents the rate of change of the drain-source voltage during device switching. It is affected by gate resistance (R_G) and parasitic capacitance. As T_J increases, R_G changes, leading to variations in dV_{DS}/dt. The turn-off voltage drops rate (dV_{DS}/dt$_{OFF}$) changes by -3.96 V/(μs·K) with T_J. However, it is highly sensitive to the bus voltage (V_{DC})—a 1% change in V_{DC} causes a 46K error in T_J. Therefore, it needs to be used in conjunction with other sensors or calibration methods [1].

Table 1 shows the selection principles of the TSEP based T_j estimation.

Table 1. TSEP Selection Principles

Selection Principle	Description
Sensitivity Priority	High-sensitivity TSEPs (e.g.$T_{D, OFF}$, $V_{DS, ON}$) are preferred for high-precision measurement scenarios. For low-sensitivity *TSEPs* (e.g.$T_{D, ON}$), combination with other TSEPs is required [1].
Robustness Requirement	Static TSEPs ($R_{DS, ON}$, $V_{DS, ON}$) have strong anti-interference capabilities. Dynamic TSEPs need improved circuits (e.g. differential amplifiers, digital isolation) to reduce noise interference [1,5].
Scenario Adaptation	$R_{DS, ON}$ is suitable for high-frequency scenarios; $V_{DS, DIODE}$ is applicable for low-current scenarios; $T_{D, OFF}$ is used for multi-chip modules (to detect hot spots) [1].

2.3. TSEP Acquisition Circuit

A specialized circuit is required to measure the four virtual TSEPs ($V_{VTH, ON}$, $T_{VD, ON}$, $V_{VTH, OFF}$, $T_{VD, OFF}$). As shown in Fig. 1, this circuit utilizes the parasitic inductance ($L_{S'S}$) of the Kelvin source to obtain voltage signals ($V_{S'S}$). It consists of two parts: one for measuring turn-on TSEPs and the other for turn-off TSEPs. A time-to-digital converter (TDC) is used to measure delay times, and a sample-and-hold circuit captures threshold voltages. The "signal (used for device control) triggers the TDC, and comparators detect when $V_{S'S}$ reaches a reference voltage (V_{REF}). This circuit can measure all four parameters within a single PWM cycle, enabling real-time measurement [7].

A dedicated circuit is needed to measure static TSEPs such as $V_{DS, ON}$ and $R_{DS, ON}$. This circuit takes the drain-source voltage and drain current of the SiC MOSFET as input signals, and uses a high-precision differential amplifier to suppress common-mode noise (e.g. Electromagnetic interference from the power loop). It consists of two core modules: a voltage sampling module and a current sampling module. The voltage sampling module uses a precision resistor divider to scale down the high-voltage $V_{DS, ON}$ to a measurable low-voltage range (0-5V), while the current sampling module adopts a shunt resistor to convert I_{DS} into a voltage signal. A 16-bit analog-to-digital converter (ADC) is used to collect the processed voltage signals, and a microcontroller unit (MCU) calculates $R_{DS, ON}$ by dividing $V_{DS, ON}$ by I_{DS}. This circuit achieves a sampling rate of up to 100 kS/s and a measurement error of less than 1% for $V_{DS, ON}$, making it suitable for steady-state TSEP monitoring [1,5].

To measure dynamic TSEPs related to gate characteristics (e.g. gate charge Q_G and gate delay time), a specialized gate charge monitoring circuit is designed. This circuit is connected in parallel with the gate-source loop of the SiC MOSFET and utilizes a low-input-impedance operational amplifier to track the gate current (I_G) in real time. It includes a current-to-voltage conversion module (converting I_G to a voltage signal V_{IG}) and an integration module (integrating V_{IG} over time to obtain Q_G). A high-speed comparator is used to detect the start and end points of the gate voltage (V_{GS}) rise/fall, thereby calculating the gate delay time (e.g.$T_{D,ON}$). The circuit uses a galvanic isolation chip to isolate the gate loop from the control loop, preventing high-voltage interference from damaging low-voltage components. It can complete Q_G and $T_{D, ON}$ measurement within 100 ns, meeting the requirement of high-speed dynamic TSEP acquisition [8].

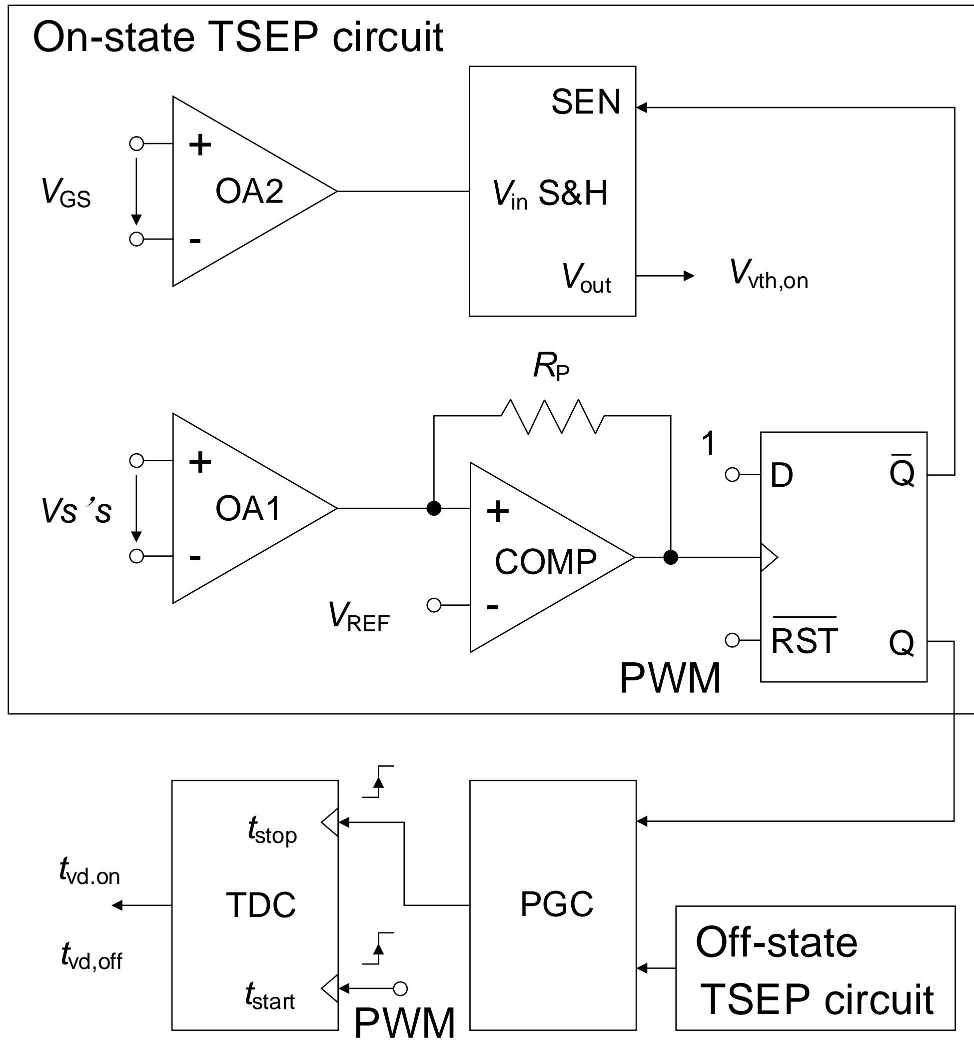

Fig. 1 Block diagram of the connection of the acquisition circuit for the TSEPs (Muñoz Barón et al., 2024) [7].

This circuit solves the problem of real-time measurement of dynamic TSEPs. It employs digital isolation to transmit signals from the high-voltage side to the low-voltage side, ensuring safety and accuracy. The reference voltage (±1.25V in the experiment) is selected to avoid false triggers and ensure it falls within the range of $V_{S'S}$ [7].

3. T_J Prediction Models Based on TSEPs

3.1. Traditional Mathematical Models

3.1 1 Polynomial Fitting Model

This model is commonly used for static TSEPs such as $V_{DS, ON}$. Since $V_{DS, ON}$ is affected by T_J, I_{DS}, and gate-source voltage (V_{GS}), a multi-variable polynomial is used to describe their relationship: $T_J = a_0 + a_1 V_{DS, ON} + a_2 I_{DS} + a_3 V_{DS, ON}^2 + a_4 I_{DS}^2 + a_5 V_{DS, ON} I_{DS}$. Here, a_0 to a_5 are coefficients obtained through experimental data fitting. For example, this model achieves an R^2 of 0.984 with actual experimental data and 0.921 with simulation data. To enhance fitting stability, researchers use the Levenberg-Marquardt algorithm, which reduces the maximum error by 20% compared to the Gauss-Newton method [3].

3.1 2 Thermal Network Fusion Model

This model combines TSEPs with thermal resistance models (e.g. RC networks). The core idea is $T_J = T_{CASE} + \Delta T_J$, where T_{CASE} is the temperature of the device case (measured by an NTC sensor) and ΔT_J is the temperature difference between the junction and the case (predicted by TSEPs). For example, when $R_{DS,\,ON}$ is used to predict ΔT_J and combined with NTC data, the measurement error at 100°C decreases from 5°C to 2°C. This model addresses the issue that TSEPs cannot accurately measure T_J when the temperature is stable [1].

3.2. Data-Driven Models

3.2.1 Back Propagation Neural Network (BPNN)

BPNN is an AI model that learns from data. It takes two inputs: the number of power cycles (to reflect device aging) and the TSEP measurement value (e.g. T_J predicted by $R_{DS,\,ON}$). The output is the actual T_J (calibrated by $V_{DS,\,DIODE}$). A BPNN with 3 hidden layers (32 nodes each) can reduce the error caused by aging from 18°C to less than 2°C. During model training, the learning rate is set to 0.001, the maximum number of iterations is 10000, and 70% of the data is used for training while 30% is used for testing [1].

3.2.2 Deep Neural Network (DNN)

DNN is well-suited for multi-chip modules. For example, in a 10-parallel ROHM BSM400D12P2G003 module, DNN takes NTC temperature (TNTC), $V_{DS,\,ON}$, $R_{DS,\,ON}$, and V_{GS} as inputs and outputs the maximum T_J (T_J -max) of the chips. A DNN with 3 layers (16×16×8 nodes) has a mean absolute error (MAE) of 0.72°C at temperatures above 125°C. For a 4-parallel Semi-power module, the MAE is 0.61°C. The use of the Levenberg-Marquardt optimizer improves model convergence—the mean squared error (MSE) decreases to 0.678 (for 4-parallel modules) and 0.991 (for 10-parallel modules) [1].

3.3. Multi-TSEP Fusion Models

3.3.1 Feature-Level Fusion

This method combines TSEPs with complementary advantages. For example, $R_{DS,\,ON}$ enables fast measurement but is affected by aging, while $V_{DS,\,DIODE}$ provides stable measurements but is slow. By calculating $T_J = 0.6 \times T_J\,(R_{DS,\,ON}) + 0.4 \times T_J\,(V_{DS,\,DIODE})$, the error after 6337 power cycles decreases from 18°C to 3°C. The weights (0.6 and 0.4) are determined based on the accuracy of each TSEP [1].

3.3.2 Model-Level Fusion

This method uses two models: a static model ($R_{DS,\,ON}$) for steady-state conditions and a dynamic model ($T_{D,\,OFF} + V_{PEAK}$) for transient conditions. A switching logic determines which model to use—for high-frequency switching (>40kHz), the dynamic model is employed (with an error of ±5K); for low-frequency steady states, the static model is used (with an error of ±2K). This ensures measurement accuracy under different operating conditions [1].

4. Engineering Challenges and Future Directions

4.1. Current Challenges

4.1.1 Parasitic Parameter Suppression

Parasitic inductance reduces the accuracy of $V_{DS,\,ON}$ measurements at high frequencies, and changes in R_G affect dynamic TSEPs. To solve these issues, Kelvin connections are used to eliminate parasitic resistance, low-pass filters reduce noise, and compensation circuits correct for R_G temperature drift [1].

4.1.2 Real-Time Calibration

Aging alters the relationship between TSEPs and T_J, requiring regular calibration. Devices from different manufacturers have varying parameters, resulting in poor model universality. Researchers are developing adaptive algorithms that update model coefficients every 1000 cycles (using $V_{DS, DIODE}$ as a reference) and building device databases to adapt models to different types via transfer learning [1,2].

4.1.3 Multi-Scenario Adaptation

At low temperatures (<25°C), the sensitivity of $R_{DS, ON}$ decreases. At high voltages (>600V), dV_{DS}/dt becomes unstable. Solutions include using $V_{DS, DIODE}$ for auxiliary measurement at low temperatures and adding V_{DS} feedback to optimize polynomial coefficients at high voltages [1].

5. Conclusion

Static TSEPs ($R_{DS, ON}$, $V_{DS, ON}$) are easy to integrate into engineering applications, while dynamic TSEPs ($T_{D, OFF}$, V_{VTH}) are suitable for high-precision transient measurements. Combining multiple TSEPs balances measurement accuracy and robustness. Data-driven models (BPNN, DNN) effectively compensate for errors caused by aging and parasitic parameters—with MAE as low as 0.61°C for multi-chip modules. Experiments show that TSEP-based methods have errors within 3°C in the range of 25-150°C, providing support for the thermal management and reliability improvement of SiC MOSFETs. Future research will focus on wider temperature ranges and integrated chips to enhance the practicality of these methods [1,7].

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