Research on Power Consumption Design Optimization of 4-Bit Absolute Value Comparator

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Abstract. This paper conducts a systematic study on the optimized design of a 4-bit absolute value comparator, focusing on its critical role in digital circuits and exploring multi-dimensional performance enhancement approaches. First, the fundamental structure of the 4-bit absolute value comparator is elaborated, including the core functions of the absolute value generation module (which converts signed numbers into absolute values) and the comparison logic module (which performs magnitude comparison of absolute values). Next, the research progress of existing optimization methods is reviewed: traditional CMOS designs achieve a balance between power consumption and delay through gate-level optimizations such as logic simplification and multi-threshold voltage (MTCMOS) techniques; adiabatic logic approaches (e.g., ECRL, PFAL) significantly reduce power consumption via energy recovery mechanisms but are limited by speed and power supply complexity; novel design strategies break through single-metric constraints by employing critical path restructuring, dynamic voltage scaling, and logic function reuse, thereby improving transmission rate, area efficiency, and reliability. Furthermore, the advantages and limitations of various methods are analyzed, including issues such as process sensitivity and scenario adaptability. Finally, the current research shortcomings and limitations are summarized, and targeted suggestions are proposed to provide a systematic reference for promoting the application of 4-bit absolute value comparators in low-power and high-performance scenarios.

Keywords. 4-bit absolute value comparator, CMOS, adiabatic logic approaches, power consumption.

1. Introduction

As the core of modern information processing systems, digital circuits play a vital role in fields such as computers, communications, consumer electronics, and embedded systems. Power consumption, area, and delay are three critical performance metrics for analyzing any digital circuit [1]. Among various fundamental functional units, comparators serve as essential modules for numerical judgment and data processing. The power consumption of a comparator significantly influences the overall power consumption of the entire circuit system.

The 4-bit comparator, being a typical circuit for small-to-medium-scale data comparison, not only reflects the fundamental design principles of basic comparators but also sufficiently demonstrates the comprehensive optimization capabilities in terms of speed, power consumption, and area [2]. As a fundamental approach to implementing bit-wise operations in logic circuits, it holds great importance for deepening the understanding of digital integrated circuits [3]. In many binary systems, such as digital electronic computers, it is often necessary to compare two binary numbers and execute subsequent operations based on the comparison results. From a broader application perspective, although the comparator is a relatively small functional unit, it plays a key role in the operation of high-performance computing systems (e.g., supercomputers). Meanwhile, in specific circuit design instances, such as temperature alarms and various sensors, comparators also perform indispensable functions [4] [5]. To accelerate computational processes in computers, it is highly useful to design a suitable device with lower energy consumption, shorter delay, and reduced component cost [6].

However, existing research in this direction still exhibits certain shortcomings: on one hand, some circuits incur excessive power consumption while pursuing high speed; on the other hand, power optimization strategies often sacrifice the balance between delay and area performance. Therefore,

exploring more efficient power optimization strategies while ensuring circuit correctness and computational accuracy has become an issue worthy of further investigation.

This paper focuses on the design optimization and performance improvement of a 4-bit absolute value comparator. Firstly, it systematically reviews recent relevant achievements to comprehensively grasp the current state of technological development in this field. Secondly, it conducts an in-depth analysis of the advantages and limitations of existing 4-bit absolute value comparator structures in terms of key metrics such as speed, area, and power consumption, identifying the core bottlenecks of current designs. Finally, with power optimization as the main focus, targeted improvement directions are proposed, striving to achieve further reduction in power consumption while ensuring reasonable circuit speed and area. This study provides a feasible reference for energy efficiency-driven digital circuit design and holds significant practical value for promoting the development of low-power and high-performance digital circuits.

2. Basic Structure of Absolute Value Comparator

An absolute value detector is a specially designed magnitude comparator. It receives signed values as inputs and outputs either 0 or 1 to indicate whether the absolute value of one input is greater than that of the other input. The basic structure of the absolute value comparator is illustrated in Fig.1 below.

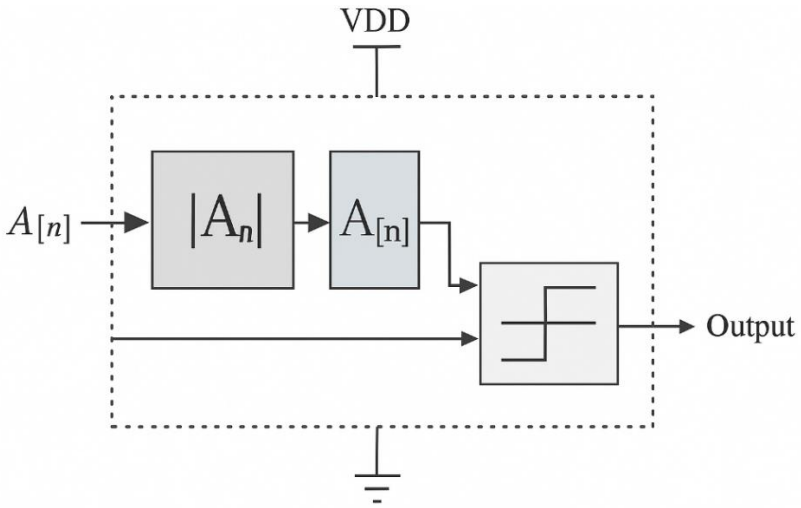

Figure 1. Basic structure of absolute value comparator

3. Circuit Models and Power Consumption Optimization Strategies

Alam et al. employed two types of partial adiabatic logic (Efficient Charge Recovery Logic, ECRL, and Positive Feedback Adiabatic Logic, PFAL) to design a 4-bit comparator circuit and compared its performance with a traditional CMOS logic-based 4-bit comparator [7]. Both adiabatic logic-designed 4-bit comparators consist of 11 gates (including XOR, AND, and NOR gates), utilizing dual-rail input and output to reduce inverter usage, thereby optimizing area and gate count. Compared to the excessive power consumption of traditional CMOS comparators, these adiabatic logic designs employ an energy recovery mechanism to minimize energy waste and significantly reduce power consumption. Simulation results show that the ECRL comparator consumes 13.64% less power than the CMOS comparator, while the PFAL comparator consumes 54.54% less. Furthermore, while ensuring the basic functionality of the 4-bit comparator (outputting A>B, A<B, and A=B signals), the adiabatic logic design achieves a balance between low power consumption and circuit performance (such as logical correctness), providing a superior solution for power-sensitive applications like portable devices.

Yu et al. implemented a hybrid design of a 4-bit absolute value detector using static CMOS logic, pass-transistor logic, and transmission gate logic [8]. This design employs the aforementioned hybrid approach to simplify the circuit and identify specific logic, particularly for the absolute value detection function, to reduce transistor count. To prevent unexpected delays caused by driving large capacitive loads at the output, the design incorporates an inverter chain as a buffer to mitigate this issue. Based on the logical effort theory, the capacitance and resistance of each gate are converted into ratios of unit-sized inverters to determine the total delay and energy consumption after identifying the critical path. This study utilizes transistor sizing and power supply scaling techniques to optimize circuit delay and energy consumption for different optimization objectives.

Li divided the 4-bit absolute value detector into an absolute value section and a comparator section [9]. The absolute value section processes the sign bit through logic gates, performs two's complement operation on negative inputs, and outputs the absolute value; the comparator section uses a subtractor and logic gates to compare the result with a threshold and output a binary signal. The optimization methods primarily include two aspects: first, analyzing the logical effort, electrical effort, and branching effort of the critical path to determine the minimum delay and adjust the gate sizes of the critical path accordingly; second, optimizing the power supply voltage VDD, with the ideal value calculated to be 0.7758 V, and performing circuit optimization at this voltage. The results show that, while ensuring performance, the total energy consumption is reduced from 49.88C at minimum delay to 32C, a reduction of approximately 40%, significantly improving energy efficiency and better meeting low-power design requirements. Compared to traditional comparator-based absolute value detectors, the optimized design features a shorter critical path and avoids the use of high-fan-in gates, thereby enhancing operational speed and stability to some extent, and providing a superior circuit foundation for the efficient operation of related systems.

4. Analysis and Discussion

4.1. Analysis and Discussion of Adiabatic Logic Circuit Design

Firstly, the experimental environment was set at a operating frequency of only 167 Hz, which significantly differs from the MHz or even GHz-level operating frequencies of practical digital circuit systems. Energy consumption evaluations at such low frequencies cannot fully reflect the circuit's performance in real-world applications. Therefore, it is necessary to conduct simulations and tests at higher frequency ranges to assess the applicability and stability of energy recovery logics under different operating conditions.

Secondly, the study only compared power consumption and transistor count, without analyzing key metrics such as circuit delay, propagation time, and Energy-Delay Product (EDP). Since delay plays a decisive role in high-speed computing and real-time signal processing, future research should integrate delay and power consumption to form a more comprehensive performance evaluation system.

Finally, the study was based on 180 nm process technology. However, as process nodes advance to 65 nm, 28 nm, and even more advanced technologies, the physical characteristics of transistors, leakage currents, and parasitic parameters will undergo significant changes, which may weaken or alter the advantages of energy recovery logics. Additionally, the practical application of PFAL and ECRL requires additional clock generation and phase control circuits, whose overhead was not accounted for in the literature. Thus, future research should validate findings at more advanced process nodes and comprehensively evaluate the actual optimization potential of comparator circuits by considering factors such as area and energy consumption of auxiliary circuits. The summarized shortcomings and improvement strategies are illustrated in Table I.

Table 1. Summary of shortcomings and proposed improvements in adiabatic logic circuit design

Shortcomings	Specific Manifestations	Optimization Suggestions
Excessively Low Operating Frequency	Experimental simulation is only conducted at 167 Hz, which is far lower than the actual MHz-GHz operating conditions.	Conduct simulation tests in the MHz-GHz frequency band and introduce indicators such as PDP to verify practical applicability.
Incomplete Evaluation Metrics	Only power consumption and the number of transistors are compared, while key indicators are not considered.	Add delay and EDP analysis and build a comprehensive performance evaluation system for power consumption, delay.
Process and System Factors Not Considered	The research is based on 180nm technology, without considering parasitic effects of advanced nodes and clock circuit overhead.	Verify under advanced processes such as 65nm, and include the power consumption and area of clock circuits in the evaluation.

4.2. Limitations Analysis and Improvement Strategies for Hybrid Circuit Designs Based on Static CMOS Logic, Pass-Transistor Logic, and Transmission Gate Logic

The model proposed by Yu et al. exhibits limitations in practical applications. It explicitly notes that adiabatic logic circuits possess the inherent drawback of slow switching [8]. This is because both ECRL and PFAL rely on four-phase pulsed power clocks to achieve energy recovery, and the clock phase switching and energy recovery processes increase signal transmission delay. For high-frequency signal processing (e.g., scenarios above the 167 Hz frequency used in the simulation), this delay may reduce data processing efficiency, making it difficult to meet the requirements of applications with high real-time demands (such as high-speed ADCs or high-frequency communication modules). In area-sensitive applications, although the transistor count of ECRL (100 transistors) is slightly lower than that of traditional CMOS comparators (116 transistors), the PFAL comparator requires 124 transistors, which is higher than that of CMOS. Moreover, both adiabatic logic types require additional circuits to generate and synchronize the four-phase pulsed power clock, potentially further increasing the actual layout area. This could lead to higher hardware costs for portable devices pursuing high integration or high-density chip designs.

Both ECRL and PFAL require a four-phase pulsed power supply, which not only complicates the design but also demands strict phase synchronization to ensure energy recovery efficiency and logical correctness. In practical systems, additional pulsed power generation circuits increase overall design complexity and may introduce issues such as clock skew and noise, reducing system stability. Simultaneously, the power consumption of the pulsed power supply may partially offset the energy savings achieved by adiabatic logic, particularly in low-load or small-scale circuits.

To address the speed bottleneck, a co-design approach using multi-threshold voltage (Multi-Vt) technology and pipeline architecture is proposed. Low-threshold transistors are used in critical paths to enhance switching speed, while high-threshold devices are employed in non-critical paths to suppress leakage current. Pipeline processing improves data throughput, compensating for single-operation delay. To mitigate area overhead, transistor-level design is optimized using a customized adiabatic logic cell library to reduce the number of devices required for the same functionality. Dynamic clock gating and global clock sharing strategies are adopted to reduce the area overhead of peripheral circuits. For system complexity, a fully integrated adiabatic power management unit (PMU) is designed to integrate four-phase clock generation and control functions into a single module, reducing clock skew and noise. An adaptive clock adjustment mechanism is introduced to dynamically adjust clock parameters based on workload, ensuring overall system energy efficiency. The summarized shortcomings and improvement strategies are illustrated in Table II.

Table 2. A comprehensive analysis of limitations and proposed enhancements for hybrid circuits integrating static CMOS, transistor, and transmission gate logics

Challenge	Primary Manifestation	Proposed Solution
Speed Bottleneck	Slow switching and high delay from 4-phase clocking; Inefficient for high-frequency processing(>167HZ)	Use Low-threshold transistors on critical paths; Improve data throughput
Area Overhead	High transistor count (e.g. PFAL; CMOS); Extra area for clock generation and sync circuit	Optimize transistor-level design; Reduce peripheral circuit area
System Complexity	Stringent clock synchronization requirement; Clock skew, noise, and stability issues	Single module for clock generation and control; Dynamically adjust parameters for efficiency

4.3. Analysis and Discussion of Traditional Comparator Circuits

The optimization method proposed by Li is based on specific transistor models and parameters, including critical path analysis, gate sizing, and supply voltage adjustment, all under the assumption of ideal transistor characteristics [9]. However, in practical semiconductor manufacturing processes, parameters such as threshold voltage and carrier mobility exhibit variability. Differences may occur between wafer batches and even across different locations on the same wafer, which can lead to discrepancies between actual circuit performance metrics—such as delay and power—and the design expectations, thereby affecting the consistency and stability of the optimization results.

Furthermore, as semiconductor technology advances to more scaled nodes (e.g., 3 nm, 2 nm), the physical characteristics and parasitic effects of transistors undergo significant changes, revealing a lack of forward adaptability for future advanced processes. When migrating to new technology nodes, substantial efforts in circuit modeling, simulation, and optimization may be required, increasing both design cost and time overhead.

In addition, the optimization in this study is targeted toward specific performance objectives, for example, reducing energy consumption at the expense of some delay. Such an approach is more suitable for scenarios with stringent power constraints and relaxed delay requirements, such as data preprocessing modules in power-sensitive portable devices. However, for applications with strict latency requirements—such as real-time signal processing or high-speed communication—this method may fail to meet the demands, limiting its applicability.

To address these challenges, process variation modeling should be introduced during the design phase by employing Statistical Timing Analysis (STA) and Monte Carlo simulation to verify circuit performance across multiple process corners. This approach ensures that the optimized circuit maintains stable and reliable performance under best-case, worst-case, and nominal conditions. Moreover, constructing parametric design models can allow circuit performance to adapt automatically to process variations. Additionally, implementing a multi-technology-node verification platform can facilitate early performance prediction across different nodes. In recent years, machine learning and data-driven methods have also emerged as promising techniques for learning delay and power characteristics from simulation data of existing technology nodes, enabling rapid adaptation to new processes and reducing repetitive optimization efforts.

Finally, establishing a multi-objective optimization framework that simultaneously considers power, delay, and area (PDA), with flexible weight adjustments according to application scenarios, is recommended. Coupling this framework with Dynamic Voltage and Frequency Scaling (DVFS) can further enable a single circuit to switch automatically between optimized modes for different operating conditions. A summary of the limitations and proposed improvements is shown in Fig. 2.

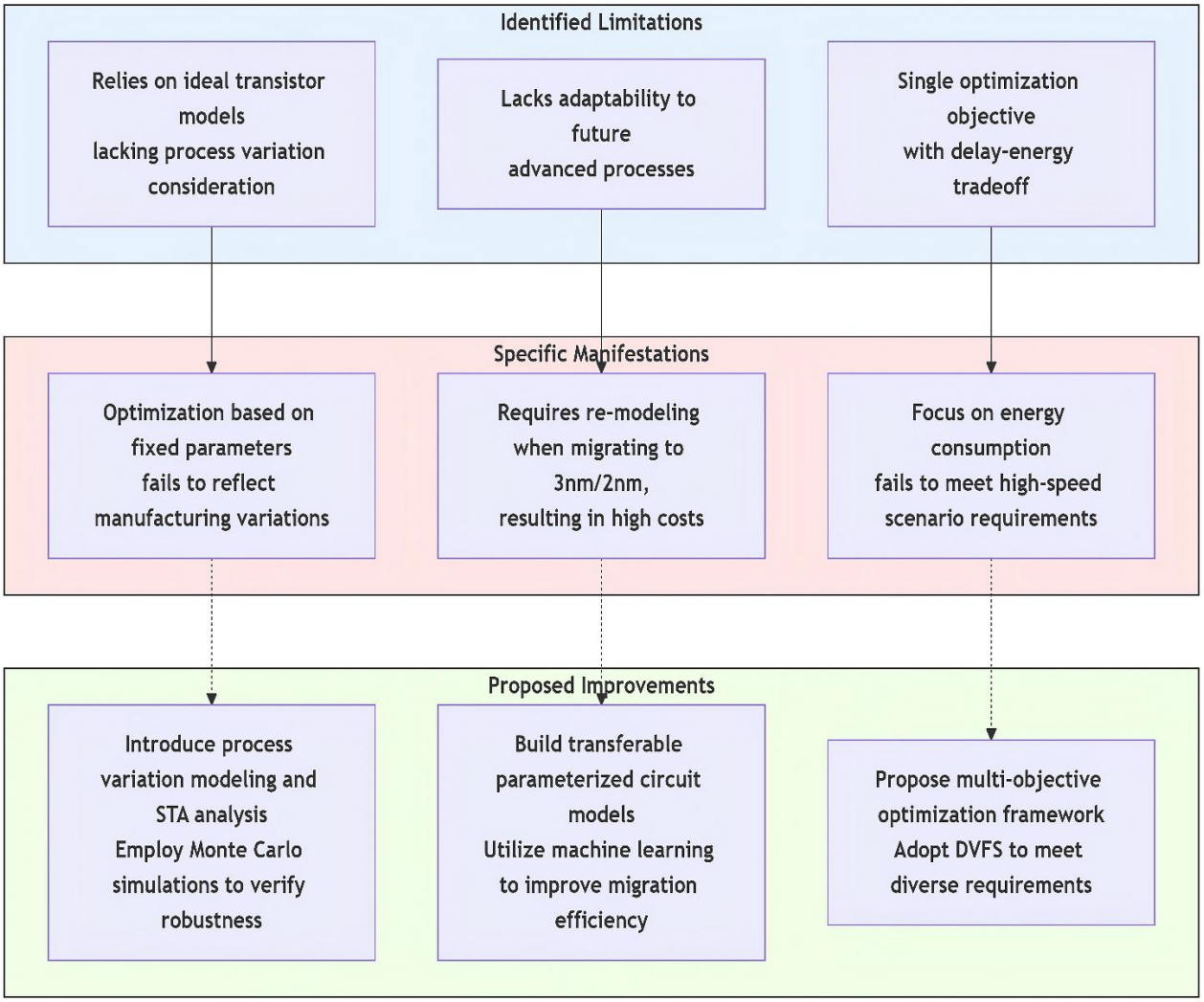

Figure 2. A summary of limitations in conventional comparator circuits and improvement recommendations

5. Conclusion

To address the common issues of increased delay, higher structural complexity, and limited process adaptability in 4-bit absolute value comparators, this paper systematically analyzes the limitations of three representative models in terms of power consumption, delay, and structural complexity, and proposes corresponding optimization strategies. The core focus of this work is on reducing critical path delay, improving overall performance, and achieving a balance between energy efficiency and integration density, in this time of rapid evolution in the digital age [10].

Building on this foundation, a comprehensive design methodology is developed that integrates logic structure reconstruction, transistor sizing optimization, and supply voltage tuning, thereby achieving a systematic improvement over conventional approaches. Unlike previous studies that optimize only a single metric (e.g., power or delay), the proposed method simultaneously considers multiple objectives and achieves significant improvements in performance, power, and area, demonstrating the necessity and forward-looking nature of system-level optimization for dedicated comparator circuits in emerging applications.

More importantly, the proposed design framework offers strong scalability and process portability, making it applicable to higher-bit comparators and other arithmetic logic units. It can effectively meet the growing demand for low power and high reliability across diverse scenarios such as AI-enabled devices, edge computing, and high-performance processors. Therefore, this research not only

introduces a novel optimization approach for academic exploration but also provides a practical technical reference for the development of energy-efficient integrated circuit design in industry.

References

[1] S. R. Venishetty and A. K. Chidra, “Design of power efficient, high-speed 4-bit comparator in UMC 180 nm technology”, Eng. Appl. Sci. Res., vol. 48, no. 1, pp. 40–47, Jan. 2021.

[2] H. Ou, Y. Liu, X. Fu, L. Huang, Y. Zhu, W. Yin, and L. Wang, "Design of a high voltage and low power comparator circuit," Microelectronics, vol. 53, no. 3, pp. 402-407, Jun. 2023. (in Chinese)

[3] X. Dong, B. Jing, and X. Yang, “Improved design of a 4-bit absolute-value detector using simplified chain carry adder,” in Journal of Physics: Conference Series, vol. 2113, Art. no. 012043, 2021.

[4] N. Trifunovic, V. Milutinovic, J. Salom, and A. Kos, “Paradigm shift in big data supercomputing: dataflow vs. controlflow,” Journal of Big Data, vol. 2, Art. no. 4, Dec. 2015.

[5] M. Ho, "Fast parallel molecular solutions for DNA-based supercomputing: The subset-product problem," Biosystems, vol. 80, no.3, pp.233–250, 2005.

[6] K. Xiao, “Upgraded Design of 4-bit Absolute-Value Detector Adopting Simplified Circuit Scheme,” in 2023 6th International Conference on Information Technologies and Electrical Engineering (ICITEE), Changde, China, pp. 1–8, Nov. 2023,

[7] S. Alam, S. R. Ghimiray, and M. Kumar, “Performance analysis of a 4-bit comparator circuit using different adiabatic logics,” in 2017 International Conference on Innovations in Power and Advanced Computing Technologies (i-PACT), Vellore, India, pp. 1–5, Apr. 2017.

[8] A. Yu, X. Zhou, and Y. Zhong, “Design and optimization of 4-bit absolute-value comparator using CMOS & PTL technique,” in 2021 International Conference on Electronic Information Engineering and Computer Science (EIECS), Changchun, China, pp. 912-916, Sep. 2021.

[9] T. Li, "Absolute value comparator structure optimization and application scenario analysis," Highlights in Science, Engineering and Technology, vol. 111, pp. 565-572, 2024.

[10] Y. Wang, "Design and analysis of 4-bit absolute-value comparator in 65nm technology using hybrid TG/CMOS," in Proceedings of the 2023 International Conference on Machine Learning and Automation, Adana, Turkey, pp. 189-199, Oct. 2023.