Impact of Power, EMI, and SET on VLSI NOR Circuits with Collaborative Hardening Approaches

Yicheng Duan

School of Electronic Engineering, Xi’an University of Posts & Telecommunications, Xi'an, China

yicheng.duan@stu.xupt.edu.cn

Abstract. Under deep submicron and nanoscale VLSI process conditions, chip reliability design has become equally critical as performance and power consumption. As a fundamental building block of SRAM, latches, and various combinational logic circuits, the stability of NOR gates directly determines the reliable operation of chips. This paper focuses on investigating the impacts of power consumption (static and dynamic), electromagnetic interference (EMI), and single-event transients (SET) on the performance of NOR circuits, analyzing both their individual effects and the coupling mechanisms under concurrent interactions. Findings reveal that excessive power consumption induces heating and compresses noise margins; EMI compromises signal integrity through coupling; and SET can trigger transient errors or even soft errors. By systematically examining the mechanisms of these phenomena in light of advanced process node characteristics, corresponding countermeasures are proposed, including circuit-level optimization, layout design methods, and system-level protection strategies. Through a comprehensive study of their synergistic effects, a cross-level, multi-dimensional collaborative design paradigm is further proposed to enhance the reliability of NOR circuits in complex environments, providing implementable theoretical support and engineering pathways for highly reliable chip design.

Keywords: NOR circuit, Power Consumption, Electromagnetic Interference (EMI), Single-Event Transients (SET), Synergistic Effects.

1. Introduction

Very-large-scale integration (VLSI), which integrates a vast number of transistors—particularly MOS devices—onto a single chip, has become a core technology widely applied in fields ranging from smartphone processors to spacecraft control systems. After more than half a century of development, its fundamental technologies have matured considerably; however, efforts to enhance performance remain unceasing. Alongside rapid advancements, new challenges and difficulties continue to emerge. In VLSI design, the NOR circuit, as one of the fundamental logic units, is widely used in memory, microprocessors, and other digital systems. As process technology enters the nanoscale, NOR circuits face numerous performance challenges, among which power consumption, electromagnetic interference (EMI), and single-event transients (SET) are key factors affecting their performance and reliability.

In space, there exists a vast number of high-energy particles (such as protons, electrons, heavy ions, etc.). The bombardment of integrated circuits by these particles can induce single-event effects. SET represents a critical failure mode, potentially leading to logic errors or even system crashes. With increasing chip operating frequencies and transistor scaling, power consumption has become a major concern, affecting not only energy efficiency and thermal management but also inducing EMI through power networks, thereby threatening peripheral circuits. Moreover, quantum effects at the nanoscale and enhanced interconnect parasitics further exacerbate EMI, imposing severe challenges to signal integrity and system stability.

In the study of power consumption, TSMC has conducted in-depth exploration of technologies to reduce power consumption under nanoscale processes. Innovations such as the N3P process continuously advance the field, significantly mitigating leakage currents through techniques including high-k dielectric metal gates. Intel, on the other hand, has adopted backside power delivery in its 18A process [1]. Regarding EMI the NOR circuits in IBM's Power10 processor utilize current-mode logic to reduce radiation intensity, while TSMC employs low-k dielectric materials in its

process technology to minimize capacitive coupling [2]. For mitigating SET, the NOR circuits in Xilinx Spartan-6 FPGAs leverage triple modular redundancy (TMR) to decrease the single-event upset cross-section. Furthermore, NASA's Mars rovers incorporate heavy-ion shielding layers for NOR circuits, substantially reducing the incidence of SET events.

This paper first reviews domestic and international research progress on the impacts of power consumption, EMI, and SET on the performance of NOR circuits in VLSI. It then conducts a systematic analysis and comparison based on the current state of technology, and finally proposes several improvement suggestions and solutions. The significance of this study lies in its integration of global research findings and industrial practices, providing multi-dimensional technical references for NOR circuit design. It supports the realization of highly reliable NOR circuits in fields such as aerospace, artificial intelligence, and the Internet of Things, thereby expanding the applications of VLSI technology and enhancing its reliability assurance.

2. NOR Circuit Characteristics

2.1. Power Consumption Impact and Low-Power Design Strategies for NOR Circuits

2.1.1. Effects of Power Consumption

Power consumption can be categorized into dynamic and static power consumption, each exerting distinct effects on NOR circuits that must be considered separately. Dynamic power consumption primarily stems from the charging and discharging of capacitive loads during circuit switching activities, significantly impacting normal circuit operation. Specific effects include:

First, elevated power consumption raises chip temperature, reducing carrier mobility, weakening the driving capability of NOR transistors, increasing propagation delay, slowing circuit speed, and ultimately limiting the maximum clock frequency [3]. Local overheating may further create hot spots, triggering hot carrier injection (HCI) and accelerating device degradation. Second, when supply voltage (VDD) is scaled down for energy saving, the reduced voltage margin lowers the noise tolerance of NOR gates. As logic levels approach the threshold voltage, circuits become more susceptible to EMI and single-event disturbances, leading to potential logic upsets.

Static power consumption primarily arises from subthreshold and gate leakage currents, exerting significant impact on circuit operation. First, it elevates overall heat generation with uneven distribution, potentially leading to local overheating. For instance, in SRAM cells constructed with NOR gates, excessive leakage current can gradually dissipate the stored charge, potentially causing data loss during standby over extended periods [4]. Moreover, static power consumption, particularly subthreshold leakage, is highly sensitive to process variations and temperature fluctuations, leading to significant differences in NOR gate leakage across different chip types, specifications, or even regions within the same chip, thereby increasing circuit performance uncertainty.

2.1.2. Low-Power Design Recommendations

To address power consumption challenges, low-power design strategies must be implemented across multiple levels, including circuit, architecture, and process, to achieve overall system optimization. At the circuit level, the following approaches can be considered:

a) Multi-Threshold Voltage (Multi-Vt) Technique: Low-threshold voltage (Low-Vt) transistors are used on critical paths of NOR circuits to ensure speed, while high-threshold voltage (High-Vt) transistors are applied on non-critical paths to significantly reduce leakage current.

b) Clock Gating: Disabling the clock signal of idle modules lowers their dynamic power consumption and simultaneously reduces the power overhead of the clock tree.

c) Clock Gating: Disabling the clock signal to idle modules reduces their dynamic power consumption and minimizes power dissipation in the clock tree.

d) Dynamic Voltage and Frequency Scaling (DVFS): Voltage and frequency are dynamically adjusted according to the workload to meet performance requirements while avoiding prolonged high-power operation.

At the architectural level, power consumption can also be optimized by design strategies such as implementing parallel processing or pipelined structures, achieving a balance between system performance and energy efficiency. Even at lower voltages and frequencies, overall computational throughput is maintained, mitigating power constraints through architectural improvements. Algorithm and state encoding optimization further reduces unnecessary switching activities in circuits, lowers the switching activity factor (α), and effectively suppresses dynamic power consumption.

At the process level, novel device architectures such as SOI (Silicon-On-Insulator) and FinFETs suppress leakage currents effectively. Their steeper subthreshold swing and enhanced gate control capability make them well suited for low-power NOR circuit design [5].

2.2. EMI Impact and Noise Immunity Design Strategies for NOR Circuits

2.2.1. Effects of EMI

EMI typically couples into circuits through power supplies, ground lines, I/O ports, or internal chip interconnects. Its primary impact on NOR circuits lies in disrupting signal transmission.

a) EMI may cause logic errors: When high-frequency noise couples into input nodes and exceeds the noise margin, it can lead to incorrect interpretation of logic states.

b) EMI can also degrade timing characteristics: When coupled onto clock or data signal lines, it may introduce jitter and glitches, resulting in failure to meet setup and hold time requirements. In NOR-based sequential logic circuits (e.g., latches), such interference can induce metastability or functional faults, and erroneous states may be latched and propagated.

c) Persistent EMI significantly reduces the signal-to-noise ratio (SNR), causing the circuit to operate in a prolonged unstable state. This not only increases the probability of immediate errors but may also accelerate device aging and performance degradation [6].

2.2.2. Noise Immunity Design Recommendations

To enhance the noise immunity of NOR circuits, measures should be taken in the following three aspects: reducing noise coupling, ensuring power supply stability, and improving the intrinsic robustness of the circuit.

a) Layout and Interconnect: Protection rings comprising P+ and N+ guard rings should be laid out around sensitive NOR circuits. Maintaining robust substrate and well contacts provides low-impedance discharge paths for noise currents, thereby isolating the circuit from external interference. For critical signals such as clocks and resets, adopting differential signaling (e.g., LVDS) effectively suppresses common-mode noise and reduces susceptibility to EMI. Shielding: Shielding against radiated coupling can be achieved by routing ground or power lines above and below critical signal traces, such as clock lines.

b) Power Supply: Uniformly distributed MOS decoupling capacitors (Decap) within the chip can provide localized charge during switching transients, thereby stabilizing the local supply voltage and suppressing noise propagation. The power delivery network (PDN) should maintain low impedance by widening and densifying power and ground lines, along with utilizing stacked multilayer interconnects, to reduce parasitic resistance and inductance.

c) Circuit Hardening: A NOR gate with Schmitt Trigger structure can be adopted, which exhibits hysteresis characteristics that effectively filter out minor glitches or slowly varying noise on input signals. Additionally, incorporating RC low-pass filters before critical nodes susceptible to interference (e.g., global reset lines) can significantly attenuate high-frequency EMI noise.

2.3. Single-Event Transient Impact and Radiation Hardening Design Strategies for NOR Circuits

2.3.1. Effects of SET

When a high-energy particle strikes the depletion region of a MOS transistor, it instantaneously generates a large number of electron-hole pairs. Under the influence of the electric field, these carriers form a transient current pulse, which constitutes the phenomenon known as a SET [7].

In CMOS NOR gates, the reverse-biased PN junction in the off-state is most susceptible to SET. When a high-energy particle strikes a turned-off PMOS transistor (typically located in the series branch), a negative voltage pulse is easily generated at the output node. Conversely, a strike on a turned-off NMOS transistor (commonly found in the parallel branch) can induce a positive voltage pulse. The width and amplitude of the pulse are primarily influenced by factors such as particle energy (Linear Energy Transfer, LET value), collected charge, node capacitance, and drive current [8]. The generated transient pulse propagates along the logic path. If the pulse width exceeds the critical sampling width of subsequent sequential elements (e.g., flip-flops), it may be captured and latched as an erroneous bit, leading to a single-event upset (SEU), i.e., a soft error. With the advancement of process technology, reduced node capacitance amplifies voltage fluctuations caused by the same amount of collected charge. Meanwhile, increased operating frequencies make even narrow pulses more likely to be captured. Consequently, NOR circuits manufactured in advanced process nodes exhibit heightened sensitivity to SETs.

2.3.2. Hardening Design Recommendations

In digital circuits, combinational logic can be hardened at the transistor level by increasing transistor dimensions or adopting folding techniques, and at the system level through redundancy methods. These approaches enhance reliability without altering the fundamental structure of the basic cells. It is recommended to begin hardening efforts with CMOS-level reinforcement before focusing on specific cells for analysis, hardening, and verification. A hardening method proposed by Tokala Vinay Reddy et al. for combinational logic cells involves duplicating the pull-up and pull-down networks of the CMOS structure. This technique leverages the recovery current generated at sensitive circuit nodes when struck by single particles to reduce the amplitude and width of SET pulses. The method was applied to harden 28nm bulk CMOS combinational cells, and its effectiveness at this technology node was experimentally validated [9].

For smaller cells, such as NAND gates, where the output is determined by two or more inputs, a single-event transient (SET) pulse occurring at an input or within the cell may require the output to restore its original value. However, the multi-input nature increases the risk of original value loss. Therefore, when hardening cells like NAND or NOR gates, it is necessary to introduce functionality similar to memory elements to maintain the correct data in the event of an SET pulse.

Fu et al. proposed a hardened NOR gate design by inserting a Muller C-element structure to maintain the original logic state when a SET event occurs within the cell [10]. At the input stage, a topology inspired by differential cascode voltage switch logic (DCVSL) was introduced. This approach not only improves switching speed but also enhances drive strength while further increasing resilience to single-event transients. The resulting NOR circuit architecture designed by the authors is illustrated below.

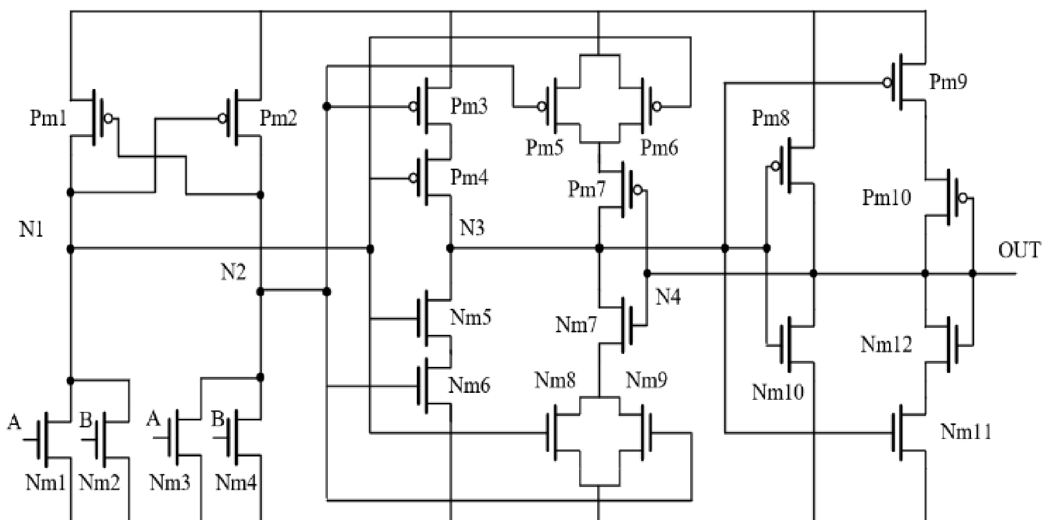

Figure 1. Structure of the NOR Circuit [10]

As illustrated in Fig. 1, the input stage of this hardened circuit employs a DCVSL gate that differs from the conventional topology [10]. Specifically, the pull-down network on one side is duplicated so that both output nodes produce the same potential, enabling logical operations to be performed at this very stage. The signals are then passed to a subsequent Muller-C element for filtering, during which the concept of duplicated pull-up and pull-down networks is applied for hardening purposes. Finally, the output stage utilizes a hardened inverter to enhance the driving capability of the cell. This architecture incorporates multiple hardening mechanisms against SET pulses and is capable of maintaining the original signal integrity even when SET pulses occur at the input or internally within the cell. However, from an energy consumption perspective, the circuit design is relatively complex, suggesting that structural optimizations could be considered while retaining its intended functionality.

For hardening combinational logic cells such as NOR gates, the objective is to either suppress the generation of pulses or glitches at their source, or to prevent the propagation or capture of disturbed signals by downstream combinational logic. The adoption of duplicated pull-up and pull-down network structures leverages the recovery current generated upon SET strikes to attenuate the amplitude and width of SET pulses, ultimately achieving enhanced radiation tolerance.

Based on the above analysis, further optimization can still be conducted from an energy consumption perspective. The architecture of the NOR circuit can be refined to reduce its energy consumption ratio while maintaining radiation tolerance. In terms of hardening, although the combinational logic cell has been reinforced, its post-hardening layout can be further optimized to reduce cell area and power dissipation. Furthermore, the functionality of various cell types can be extended to enhance the overall versatility of the cell library.

In light of the above discussion, Table I summarizes the core impacts of the three influencing factors and provides corresponding recommendations.

Table 1. Core Impacts and Corresponding Recommendations for Power Consumption, EMI, and SET

Influencing factors	Core Impacts	Key Mitigation Strategies
Power Consumption	Dynamic: Performance degradation due to heating; reduced noise margin. Static: Data loss caused by leakage current; performance fluctuation sensitive to process variations.	**Circuit:** Multi-Vt technology, power/clock gating, DVFS. **Architecture:** Parallel/pipeline design. **Process:** SOI/FinFET
Electromagnetic Interference (EMI)	Logic errors; timing violations (jitter/glitch); long-term aging.	**Layout:** Guard rings, differential signaling (e.g., LVDS), shielding. **Power:** Decoupling capacitors (Decap), low-impedance PDN. **Circuit:** Schmitt trigger, RC filtering.
Single-Event Transient (SET)	Transient pulse generation; error propagation (SEU); increased sensitivity in advanced nodes.	**Circuit:** Transistor sizing, duplicated pull-up/pull-down networks, Muller-C element insertion. **System:** Redundancy and verification. **Co-optimization:** Balancing energy efficiency and radiation tolerance.

3. Synergistic Effects and Cross-Layer Co-Design Methodology

Power consumption, EMI, and SET are not independent issues; rather, they form a complex system of interrelated and mutually influential factors, manifested in the following aspects:

Low Voltage vs. Reliability Paradox: Reducing VDD is the most effective method to decrease dynamic power consumption, but it directly diminishes noise margins, making circuits more susceptible to both EMI and SET.

Thermal-Electrical-Radiation Coupling: High power consumption leads to elevated temperatures, which alter transistor characteristics—potentially increasing leakage current (thereby further raising temperature and power consumption)—and affect charge collection efficiency during SET events, complicating error rate prediction [11].

Negative Impacts of Hardening Strategies: Most hardening techniques (e.g., TMR, filtering) introduce additional area, power, and latency overhead. These trade-offs can, in turn, exacerbate power and thermal issues and may create new sources of or sensitivity to EMI, thereby adding complexity rather than simplifying the design process.

Therefore, single-dimensional optimization is no longer sufficient to meet future requirements. A multi-level perspective is essential to address these challenges. A cross-layer co-design approach should be adopted to holistically consider the impacts of power consumption, EMI, and SET, enabling the proposal of synergistic multi-level solutions, as illustrated in Fig. 2.

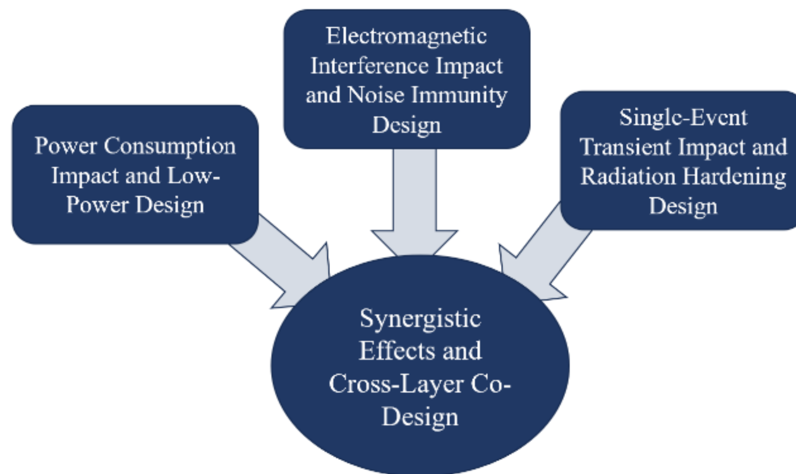

Figure 2. Framework of Synergistic Effects and Cross-Layer Co-Design

Therefore, based on the foregoing analysis, the following specific recommendations are proposed:

Collaborative optimization involves simultaneously considering performance, power consumption, reliability, and cost objectives during the early design stages. When selecting low-power technologies, it is essential to concurrently evaluate their impact on reliability and proactively incorporate necessary hardening measures [12]. Adaptive systems monitor operational parameters such as temperature, voltage, and error rates to implement adaptive voltage scaling (AVS) and adaptive body biasing (ABB). These techniques dynamically adjust operating points to ensure sufficient noise margins while enabling the dynamic activation or deactivation of redundant modules to balance reliability and power efficiency.

Design flow and EDA tools: New EDA tools and design methodologies are being developed to enable co-simulation and optimization of multi-physics effects (electrical, thermal, and radiation). These tools allow accurate prediction and evaluation of circuit reliability at the design stage, even extending to the planning and forecasting of circuit practicality in future applications [13].

4. Conclusion

VLSI technology has experienced rapid advancement, and under nanoscale process nodes, the reliability of chip design has become a key issue in ensuring robust system performance. As one of the most fundamental components in digital circuits, the stability of the NOR gate is closely tied to the reliable operation of the entire system. This paper analyzes the performance of NOR circuits from three perspectives: power consumption (including both static and dynamic), EMI, and SET effects. Each factor is examined in detail, followed by a summary of insights and proposed countermeasures. The study investigates not only the individual impact of each factor but also their synergistic interactions and the concept of cross-layer co-design. For instance, excessive power consumption leads

to temperature rise, which reduces noise margins, while EMI degrades signal integrity through coupling interference. In response, adaptive systems can be introduced to dynamically adjust circuit operating parameters, thereby balancing performance and power efficiency. Furthermore, overheating induced by high power consumption may exacerbate SET effects, giving rise to transient errors or even soft errors. Hence, it is imperative to develop new EDA tools capable of simulating, analyzing, evaluating, and predicting circuit behavior to support high-reliability design.

Moreover, this paper argues that only through multi-perspective and multi-level collaborative design strategies can the reliability of NOR circuits in complex environments be effectively enhanced. This approach provides actionable theoretical foundations and practical pathways for highly reliable chip design, thereby laying the groundwork for greater robustness and accelerated development of higher-level circuits.

References

[1] Z. Tan, L. Zhao, J. Wang, et al. “Interfacial and electrical properties of HfAlO/GaSb metal-oxide-semiconductor capacitors with sulfur passivation”. Chinese Physics B, 2014, 23 (01):431-435.

[2] P. Xu and Z. Pan, "Collaborative Applying the Ultra-low-k Dielectric and the High-k Dielectric Materials for Performance Enhancement in Coupled Multilayer Graphene Nanoribbon Interconnects," IEEE Journal of the Electron Devices Society, vol. 8, pp. 200-212, 2020.

[3] S. G. Narendra and A. P. Chandrakasan, “A. Leakage Dependence on Input Vector,” in Leakage in Nanometer CMOS Technologies, vol. II, S. G. Narendra, Y. Ye, S. Borkar, V. De, A. Chandrakasan, Eds. Boston, MA: Springer, 2006, pp.21-39.

[4] N. S. Kim et al., "Leakage current: Moore's law meets static power," in Computer, vol. 36, no. 12, pp. 68-75, Dec. 2003.

[5] Y. Wang, F. Liu, Y. Cao, et al. “Reliability study and modelling development of FinFET devices,” 2025, 25 (05): 66-74. (in Chinese)

[6] J. M. Redouté, M. Steyaert, EMC of Analog Integrated Circuits. Dordrecht: Springer, 2010.

[7] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," IEEE Transactions on Nuclear Science, vol. 50, no. 3, pp. 583-602, Jun. 2003.

[8] P. Roche, J. L. Autran, G. Gasiot and D. Munteanu, "Technology downscaling worsening radiation effects in bulk: SOI to the rescue," in 2013 IEEE International Electron Devices Meeting, Washington, DC, USA, pp. 766-769., Dec. 2013

[9] Reddy T V, Nakhate S. Radiation hardened by design technique to mitigate single event transients in combinational logic circuits [C]. 2017 International Conference on Recent Innovations in Signal processing and Embedded Systems (RISE), Bhopal, India, pp. 342-347, 2017.

[10] M. Fu. “Research on Radiation Hardening Technology Base on 28nm CMOS Integrated Circuit ,” M.S. thesis, University of Electronic Science and Technology of China, Chendu, China, 2024. (in Chinese)

[11] J. D. Black, P. E. Dodd and K. M. Warren, "Physics of Multiple-Node Charge Collection and Impacts on Single-Event Characterization and Soft Error Rate Prediction," IEEE Transactions on Nuclear Science, vol. 60, no. 3, pp. 1836-1851, Jun. 2013.

[12] S. S. Sapatnekar, "Overcoming Variations in Nanometer-Scale Technologies," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 1, no. 1, pp. 5-18, Mar. 2011.

[13] H. Xiang. “Research and Design of Thermodynamic Simulation and Optimization Methods in Multi-Physical Field Co-simulation,” M.S. thesis, University of Electronic Science and Technology of China, Chengdu, China ,2025. (in Chinese)