Research on Power Consumption and Reliability of Digital Circuits Based on CMOS Electrical Characteristics

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Abstract. This paper focuses on the evolution and optimization of CMOS devices, systematically reviewing the core characteristics of three typical device architectures: planar MOS devices, FinFETs, and MBCFETs. Subsequently, an in-depth analysis is conducted: planar MOS devices achieve switching by regulating carrier concentration via the electric field effect and are widely used in digital and analog circuits; FinFETs face challenges such as surging power consumption and declining reliability during scaling, and optimization suggestions are proposed from four aspects—low-power design, exploration of new material processes, architectural innovation, and establishment of a collaborative evaluation system; MBCFETs adopt a gate-all-around (GAA) architecture with a multi-layer channel stacking structure, offering more comprehensive gate wrapping and significant advantages in current drive capability and reduced parasitic capacitance, yet they also confront challenges such as epitaxial growth defects and increased complexity in the replacement metal gate (RMG) process. Furthermore, the article compares the performance and limitations of these three devices in a tabular format. The study elucidates the technological logic behind the evolution of CMOS from planar to 3D architectures, providing references on device characteristics for the semiconductor industry and aiding in understanding the application boundaries of different structures.

Keywords: CMOS devices, planar MOS devices, FinFET, MBCFET.

1. Introduction

Complementary pairs of p-type and n-type MOSFETs form the building blocks of CMOS architecture. The CMOS structure is adopted to achieve low power consumption, high noise margin, and scalability. By utilizing both hole and electron charge carriers, CMOS enables minimal power dissipation, consuming virtually no power when not actively switching [1]. As a traditional chip design technology, MOSFETs also exhibit several significant drawbacks. For instance, the on-state resistance of a MOSFET is typically relatively high, which can lead to substantial power consumption in high-power applications, particularly in high-voltage scenarios where conduction losses are notable. Additionally, their manufacturing costs are high, and the large on-state resistance limits their use in certain high-voltage and high-current applications.

Since its inception in the early 1970s, the development of planar CMOS technology over the past five decades has been guided by two fundamental principles: Gordon Moore′s empirical economic law and the technical principle of scaling—beginning with Robert Dennard′s theory of geometrical scaling (Dennard Scaling), followed later by equivalent scaling [2]. Geometric scaling is designed to continually shrink both the horizontal and vertical sizes of CMOS transistors while enhancing their electrical characteristics, thereby boosting the packing density and overall performance—including speed, power efficiency, and reliability—of both logic and memory devices. This process involves scaling the physical dimensions of transistor elements once a specific electrical parameter, typically either electric-field strength or supply voltage, is held constant [3]. Equivalent scaling enhances the performance of CMOS devices and integrated circuits through the adoption of novel materials, process technologies, and integration architectures—rather than by modifying the characteristic geometry of the transistors. It can be applied either independently of geometric scaling or in combination with it, with both approaches complementing each other [4]. However, like any exponential development law reliant on finite resources, Moore’s Law could not be sustained indefinitely, as certain limits were continually encountered. Only through the evolution of field-effect transistor design and improvements in manufacturing processes has the validity of Moore′s Law been extended for several more generations.

This paper centers on the evolution and optimization of CMOS devices, systematically reviewing the key characteristics of three representative transistor structures in technological development—Planar MOS, FinFET, and MBCFET (Multi-Bridge Channel Field-Effect Transistor)—and exploring their roles in performance enhancement. First, the three device types are summarized, and their basic structures are introduced with illustrations. Subsequently, each device is analyzed in detail: Planar MOS offers clear operational principles and is widely used in digital and analog circuits, but it is limited by short-channel effects at deep submicron scales; FinFET outperforms Planar MOS in dimensional scaling but still faces challenges in power consumption control and process complexity, necessitating further exploration in low-power design, material improvements, and architectural optimization; MBCFET demonstrates potential in gate control capability and power management due to its multi-bridge channel design, though its manufacturing processes and reliability require further refinement. Finally, by comparing the performance metrics and limitations of the three device types, their characteristic differences and applicable scenarios are summarized. In conclusion, this study provides a reference for understanding the evolution of CMOS technology and the advantages of different structures, offering guidance for the design and application of semiconductor devices.

2. Evolution of CMOS Devices

As shown in Fig. 1(a), the planar MOS device, being a conventional structure, features a flat channel located on the substrate surface with a gate electrode covering above. Its structure is relatively simple, but as process technology scales down, its current control capability becomes somewhat limited. In Fig. 1(b), the FinFET has a fin-shaped channel that protrudes vertically, and the gate wraps around the channel from both sides, effectively enhancing current control, mitigating short-channel effects, improving device performance, and optimizing power consumption. As a result, it is widely adopted in advanced technology nodes. In Fig. 1(c), the MBCFET employs a multi-bridge channel structure, allowing more comprehensive gate wrapping. This further optimizes current control while also increasing integration density and overall performance.

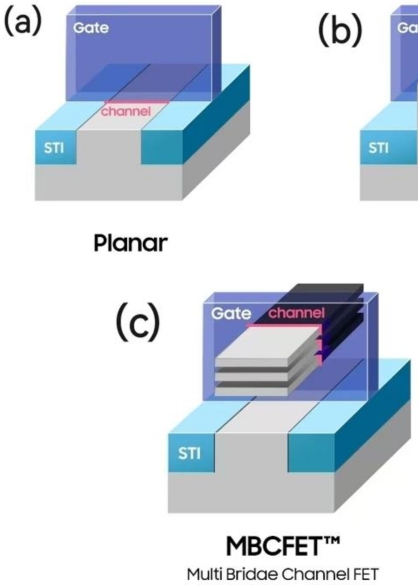

Figure 1. Classic planar field-effect transistor on a bulk silicon substrate; (b) 3D structure of dual gate FinFET; (c) Multi Bridge Channel FET

2.1. Planar MOS Device

The planar MOS device is the core structure of the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), primarily functioning as a switch or an amplifier. Its fundamental operating principle is based on the field effect, whereby the gate voltage regulates the concentration of charge carriers in the channel to switch between the "ON" and "OFF" states. In digital integrated circuits such as logic and memory devices, the MOSFET is mainly used as a switch (i.e., ON when the gate voltage is high, and OFF when it is low) or as a logic gate to perform Boolean operations. In analog ICs, it serves as a transconductor for signal amplification and conversion [5]. For many years, silicon technology has been driven by the scaling down of MOSFET dimensions to enable high-performance integrated digital circuits [6]. Planar MOS devices have been the foundation of integrated circuits for the past half-century. However, at ultra-deep submicron process nodes, they face issues such as reduced gate control capability, increased leakage current, and performance fluctuations. These limitations primarily stem from the weakened gate control over the channel in the two-dimensional planar structure as dimensions shrink, leading to device threshold voltage drift, degradation of subthreshold swing, and increased static power consumption. Recently, however, further miniaturization of MOSFETs has become critically challenging due to intrinsic limitations such as short-channel effects (SCE). In response to this issue, the following recommendations are proposed:

1) Adopt multi-gate structures (such as FinFET). Multi-gate architectures significantly enhance gate control over the channel by increasing the contact area between the gate electrode and the channel, thereby effectively suppressing short-channel effects.

2) Develop gate-all-around (GAA) structures. The GAA architecture enables three-dimensional electrostatic control of the channel by completely surrounding it with the gate material.

3) Introduce high-mobility channel materials:

For instance, using materials with high carrier mobility such as germanium (Ge) and III-V compounds (e.g., InGaAs) as the channel can further enhance device drive current and switching speed, mitigating performance degradation caused by voltage scaling.

2.2. FinFET Semiconductor Device

In traditional transistor structures, the gate that controls the current flow can only regulate the circuit′s switching (on/off state) from one side, representing a planar architecture. In the FinFET structure, the gate features a fin-like, fork-shaped 3D design, enabling control over the circuit's conduction and interruption from both sides. In the FinFET architecture, the gate adopts a fin-like, forked 3D structure that enables control over the circuit's conduction and interruption from both sides. The reduction in channel size, along with the consequent increase in chip density and operating frequency, highlights power consumption as a major challenge in nanoscale circuits [7]. As indicated in the aforementioned research, the FinFET architecture influences power consumption in nanoscale circuits due to changes in channel size, chip density, and operating frequency. Consequently, the need to optimize chip power consumption has made low-power design an essential technology required by the semiconductor industry [8]. The relentless pursuit of scaling has reduced metal-oxide-semiconductor field-effect transistors (MOSFETs) to nanoscale dimensions, significantly altering key electrical parameters including threshold voltage and on/off-state currents. These dimensional changes, driven by continuous scaling, directly influence current switching behavior—leading to heightened leakage issues and greater process variations that ultimately constrain MOSFET performance and reliability [9]. Additionally, short-channel effects in modern MOSFETs introduce several leakage mechanisms, such as reverse-biased p-n junction leakage, weak inversion leakage, and drain-induced barrier lowering (DIBL) leakage [10]. In CMOS circuits, multiple mechanisms contribute to power consumption [11]. As devices continue to scale down, the relative significance of these different components in power consumption has also shifted. For planar CMOS, which relies on single-side gate control, the reduction of device sizes to the nanoscale leads to severe short-channel effects, including a dramatic increase in leakage current and instability in threshold voltage. In contrast, the dual-side gate control in FinFETs results in a more uniform channel potential distribution, improved subthreshold swing, enhanced ON/OFF current ratio, as well as significantly higher chip density and operating frequency [7]. A core challenge common to the development of semiconductor devices such as FinFETs and MOSFETs is that, as device sizes continue to shrink (continuous scaling) in pursuit of higher chip density and operating frequency, they all face cascading issues caused by structural and parametric changes. These are manifested as significantly increased power consumption (e.g., elevated leakage current), intensified process variations, and ultimately constrained device performance and degraded reliability. Both types of devices have encountered bottlenecks in power efficiency and reliability due to the development path of scaling for performance gains. To address these common issues, the following recommendations are proposed:

1) Strengthen research and development in low-power design technologies. Leverage the structural characteristics of FinFETs and MOSFETs to optimize circuit architectures and operating modes, reducing power consumption in high-frequency and high-density scenarios.

2) Explore new materials and processes, such as adopting low-leakage materials to replace conventional semiconductors, or utilizing advanced manufacturing techniques to mitigate process variations introduced by scaling, thereby enhancing device stability.

3) Promote innovation in device architectures. Further optimize existing 3D structures (e.g., FinFETs) to balance the relationship between size, density, frequency, and power consumption—for instance, by developing more efficient gate control mechanisms to reduce leakage current.

4) Establish a co-evaluation framework for power consumption and reliability in nanoscale devices. Incorporate early-stage predictions of power and process variation impacts during design to avoid performance and reliability risks in later stages.

The following Table 1 is a brief summary of the architecture, challenges, and proposed solutions for FinFET devices.

Table 1. Summary of FINFET Device Content

FinFET		
Architecture	**Problem**	**Solution suggestions**
The gate is designed with a fork shaped 3D architecture resembling a fish fin, which can control the connection and disconnection of circuits on both sides of the circuit	Significant increase in power consumption (such as increased leakage current), unstable threshold voltage, and intensified process changes	Strengthening the research and development of low-power design technology by combining the structural characteristics of FinFET and MOSFET
		Explore new materials and processes
		Promote innovation in device architecture and balance the relationship between size, density, frequency, and power consumption
		Balance the relationship between size, density, frequency, and power consumption

2.3. MBCFET Devices

The GAA MBC-FET (Gate-All-Around Multi-Bridge Channel Field-Effect Transistor) represents an ultimate multi-channel solution where each channel is fully surrounded by the gate on all four sides, forming the "GAA" structure illustrated in Fig. 1(c). Thanks to its multi-channel design, the MBC-FET offers a larger effective channel width, which reduces resistance and enables higher current drive capability. This contributes to improved device performance, such as faster switching speeds and lower power consumption. Compared to existing FinFET technology, these novel structures can achieve higher speed performance while maintaining the same device footprint without requiring additional area [11]. One of the unique processes in MBCFET fabrication involves stacking silicon and sacrificial layers during channel formation. Horizontally positioned nanosheet channels, referred to as MBC (Multi-Bridge Channel) formation, are easily created by removing the sacrificial layers. After MBC formation, an empty space is formed between the nanosheets, known as the vertical space, as illustrated in Fig. 2 [12]. Following MBC formation, various patterning processes are carried out. During these steps, multiple materials—including pattern masks and gate materials—are deposited and subsequently removed from the vertical space region.

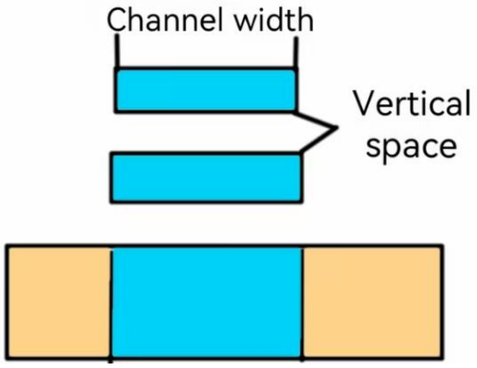

Figure 2. Vertical spatial structure diagram after MBC formation

The unique structure of MBCFET, including the application of internal spacers and the reduction of vertical space, has a profound impact on capacitance. However, the implementation of internal spacers leads to side effects such as epitaxial growth defects, while the reduction of vertical space increases the difficulty of the RMG process. Therefore, determining the appropriate scheme and dimensions is crucial for ensuring the mass production and performance of MBCFET. It is necessary to achieve a balance between performance, reliability, and yield through collaborative design and process debugging. MBCFET has a GAA structure, which offers superior gate controllability compared to FinFET, and the current flow plane is parallel to the substrate. This reduces gate extension. It is expected that before the gate extension is completely reduced to 0, there will be no significant loss in gate control, and the parasitic capacitance between the gate and S/D can be reduced. This is considered the final preferred structure of MBCFET, which not only reduces the cell height in structure but also improves performance. Although MBCFET excels in electrostatic control and power optimization, its complex three-dimensional structure and material systems still face multiple challenges. First, the stacked nanosheet and full-wrap-around gate structure of GAA MBCFET impose high requirements on photolithography, etching, and material deposition, leading to complex manufacturing processes and yield challenges. Second, the nanoscale channels and multi-layer stacking design lead to heat concentration, resulting in significant self-heating effects (SHE). To address these shortcomings, the following suggestions are proposed:

1) Process optimization and equipment upgrades can adopt high-numerical-aperture EUV (NA EUV) to improve the patterning accuracy of nanowires/nanofilms, combined with self-aligned multiple patterning (SAQP) to reduce edge roughness.

2) Innovative thermal management architecture, such as embedding microchannels (e.g., liquid cooling manifolds) within the chip, combined with metal-semiconductor thermal interface materials (e.g., graphene), can reduce thermal resistance by more than 40%.

3) Innovation in Materials and Integration Pathways: Explore novel channel materials such as two-dimensional materials (e.g., MoS_2) or strained silicon to further enhance carrier mobility and reduce power consumption;

4) Design-Technology Co-Optimization (DTCO): Use multi-physics simulation platforms (e.g., combining TCAD and compact models) to evaluate the impact of different dimensional options on electrothermal performance in advance, establish reliability-oriented design rules, and accelerate the determination of process windows and production transfer.

The following Table 2 is a brief summary of the architecture, challenges, and proposed solutions for MBCFET devices.

Table 2. Summary of MBCFET Device Content

MBCFET		
Architecture	**Problem**	**Solution suggestions**
Each channel is surrounded by gates on all four sides, forming a GAA structure. The application of internal spacers and the relative reduction of vertical space	Extremely high requirements are required for photolithography, etching, and material deposition. Significant SHE.	Optimize processes and upgrade equipment
		Innovate the cooling architecture
		Innovative Materials and Integration Path
		Collaborative optimization design and process

3. Summary of Device Performance, Limitations, and Recommendations

In Table 3, a brief summary of the performance, shortcomings, and limitations of the three types of transistor structures discussed in this article is provided. Planar MOS devices exhibit high current tolerance and reliability, but suffer from high on-resistance and significant switching losses. FinFET devices, with their multi-gate characteristics, can suppress short-channel effects and reduce leakage current; however, as dimensions shrink, they face reliability issues such as SHE and negative temperature bias instability (NTBI). The unique structure of MBCFET devices optimizes capacitance, yet challenges remain including epitaxial growth defects and increased complexity in the RMG process.

Table 3. Comparison of Performance and Limitations of Planar MOS, FinFET, and MBCFET

Type	**Performance**	**Shortcomings and limitations**
Planar MOS	Current surge tolerance and high reliability	High on-resistance and significant switching losses
FinFET	The multi-gate characteristics suppress short-channel effects and reduce the off-state leakage current faced by planar MOSFETs.	In FinFET technology, the continuous scaling of device dimensions has introduced a series of reliability challenges, including SHE and NBTI
MBCFET	The unique structure, through the application of inner spacers and reduction of vertical space, has profoundly influenced the capacitance characteristics.	The implementation of inner spacers can lead to side effects such as epitaxial growth defects, while the reduction of vertical space increases the complexity of the RMG process.

4. Conclusion

The study reveals a common challenge in semiconductor device scaling: as device dimensions continue to shrink in pursuit of higher density and operating frequency, issues such as surging power consumption (e.g., increased leakage current) and intensified process variations consistently emerge, ultimately limiting performance gains and reliability. To address this core challenge, this paper proposes the following optimization directions: strengthen research on low-power circuit architectures and operating modes tailored to device structures to reduce power consumption in high-frequency and high-density scenarios; explore low-leakage materials and advanced manufacturing processes to mitigate process variations induced by scaling; promote architectural innovations based on 3D structures, such as optimizing gate control mechanisms to reduce leakage current; and establish a collaborative evaluation system for power consumption and reliability in nanoscale devices to anticipate risks at the early design stage.

In summary, the evolution of CMOS devices has consistently followed a logic of structural optimization → performance enhancement → problem resolution. The technological progression from planar devices to FinFETs and then to MBCFETs reflects a clear developmental trend: transitioning from single-side to multi-side gate control, and from planar to three-dimensional architectures. Looking forward, the combination of material innovations, process optimizations, and architectural advancements is expected to overcome current bottlenecks and drive semiconductor devices toward higher performance, lower power consumption, and improved reliability.

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