Research Progress on Chemical Vapor Deposition for Contact Hole Processes

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Abstract. Contact holes are critical interconnect structures in semiconductor devices, and the shape and composition of the materials that fill their interiors significantly impact devices performance. Traditional deposition methods like physical vapor deposition have been replaced by chemical vapor deposition due to the poor step coverage capability. However, depositing contacts with high aspect ratios becomes increasingly challenging as device dimensions shrink. As a result, the manufacturing processes impose higher demands on chemical vapor deposition technologies for material deposition. This paper explores the development of deposition techniques for filling vias. It first introduces tungsten CVD, which is the most widely used. Besides, it presents further advanced techniques such as atomic layer deposition and selective deposition. This paper analyzes the principles, advantages, and limitations of these techniques. After that, it compares their differences in cost and other aspects. Finally, it presents the other application scenarios of these CVD techniques. The conclusion points out that tungsten CVD can improve the device performance by depositing thinner barrier layers through atomic layer deposition. Nevertheless, selective deposition eliminates the need for these layers, thus resolving high-resistance issues fundamentally. Selective deposition is a key technique for overcoming contact resistance bottlenecks.

Keywords: Contact hole; chemical vapor deposition; atomic layer deposition; selective deposition.

1. Introduction

In integrated circuit manufacturing, contact holes serve as critical structures connecting the active regions of the silicon substrate to the first metal layer. Acting as the primary bridge for electrons flowing out of the device, they significantly impact on the chip's power consumption and performance characteristics. At present, with breakthroughs in Gate-All-Around technology, Very Large-Scale Integration has entered the angstrom scale [1]. As device dimensions shrink, the aspect ratio becomes higher. At small feature sizes, the proportion of interfacial resistance in contact holes increases. Meanwhile, a high aspect ratio leads to the formation of voids. As a result, reducing contact resistance and improving step coverage ability in via processes are critical.

Early physical techniques such as vacuum evaporation and sputtering struggled to meet the demands of integrated circuit manufacturing. Consequently, CVD technologies emerged and rapidly advanced, finding extensive applications in fields like semiconductors. Compared to PVD, CVD operates at lower temperatures, offers superior uniformity in film deposition, and can be used to prepare thin films of nearly all materials in integrated circuit processes. It also exhibits excellent step coverage, making it the mainstream method for contact hole deposition [2]. Improving this technology is crucial for enhancing deposition quality. Early CVD technologies for contact holes primarily employ non-selective tungsten deposition, resulting in titanium nitride barrier layers with high impurities, high contact resistance, and numerous associated issues [3]. Moreover, traditional photolithography techniques are increasingly unable to meet the demands of ever-shrinking feature sizes, thus needing further research into smaller via processes.

This paper presents an overview of the fundamental principles of CVD technology. Subsequently, it analyzes recent advancements in its application with contact holes fabrication processes. The paper summarizes and evaluates the differences among various techniques across multiple dimensions, including process complexity and cost. Furthermore, it identifies and examines the shortcomings

inherent in these technologies along with their underlying causes. Finally, the paper outlines the application scenes and prospects of the CVD processes.

2. Main Steps of CVD

CVD is a process that deposits a thin film onto a substrate through chemical reactions involving gaseous substances. As shown in Fig.1, CVD typically involves the following steps.

Gas-phase reactants enter the reaction chamber through the gas entrance carried by carrier gas such as nitrogen. Then they diffuse through the boundary layer to the substrate surface. Once reaching the surface, the gas-phase reactants are adsorbed onto the substrate. Under ideal conditions, they can achieve uniform adsorption. After that, reactants experience various chemical reactions on the substrate surface, such as pyrolysis or redox reactions. These reactions produce gas-phase molecules that form the film and byproducts. This process requires precise control of parameters like temperature and pressure. Next, gas-phase film molecules undergo nucleation and growth on the substrate surface, gradually depositing to form a solid-state film. The byproducts desorb from the surface and are subsequently released as exhaust gas. During this process, environmental pollution must be minimized as much as possible. After deposition, further steps are required, such as improving film quality through annealing and adjusting film thickness and flatness by chemical mechanical polishing [4]. The deposition rate is determined by the gas phase transport rate and the chemical reaction rate.

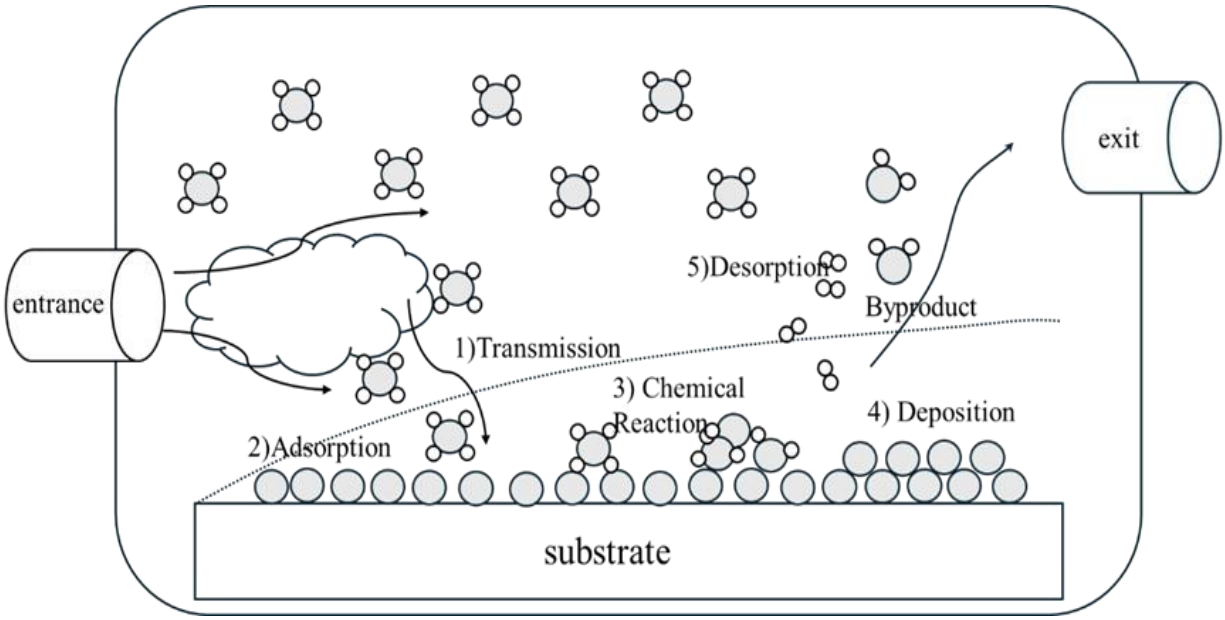


Fig 1. Main steps of CVD.

3. Fabrication Method of Contact Holes by CVD

3.1. Tungsten CVD

Tungsten CVD is a two-step process which involves nucleation and bulk deposition. The primary reactants are the tungsten precursor (WF_6) and the reducing agents (H_2, SiH_4) [5]. During the nucleation stage, WF_6 reacts with SiH_4 at low temperatures (300°C–400°C) and low pressure to form a thin and dense tungsten layer. Subsequently, in the bulk deposition stage, the temperature is increased (above 400°C) to enable WF_6 to rapidly react with H_2. The key parameters for tungsten CVD include temperature, pressure, and gas ratios [6]. During nucleation, low temperatures can curb gas-phase nucleation. In the bulk deposition stage, raised temperatures can accelerate the deposition rate. The low-temperature environment significantly reduces the probability of gas-phase nucleation. An excessively high gas radio of WF_6 to SiH_4 results in an undesirable tungsten layer during the

nucleation stage, leading to subsequent deposition with voids [7]. Conversely, an excessively low ratio causes an overload of silicon impurities.

Tungsten CVD for silicon processes offers advantages such as excellent fill capability, step coverage, and fast deposition rates. However, its precursor WF_6 and byproduct HF are highly corrosive, necessitating isolation by a titanium nitride barrier layer. Afterwards, chemical mechanical polishing is required to remove excess tungsten and achieve a smooth surface, which increases the cost of the process.

3.2. Selective Tungsten Deposition

The reduction in feature size implies that vias are becoming increasingly smaller. Traditional tungsten CVD requires the deposition of a titanium nitride barrier layer to prevent corrosion of the underlying material by WF_6. At the 7nm node, the contact hole with a diameter of approximately 20nm has its barrier layer and nucleation film occupies about 75% of the space. Consequently, the subsequently deposited tungsten metal layer becomes extremely narrow. The resulting increase in contact resistance leads to higher chip power consumption and reduced performance [8]. Selective tungsten deposition avoids coating the remaining surfaces by selectively depositing tungsten metal onto designated, pretreated areas [9]. Selective tungsten deposition primarily involves two steps. First, contaminants and oxide layers on the substrate surface must be cleaned using a plasma of H_2, N_2, etc. [10]. Subsequently, inhibitory chemicals (such as thiols and acetylenes) are employed to form a suppression layer on the non-deposition area surface, preventing the reaction and deposition of tungsten precursors on that surface. The clean silicon surface is then coated with tungsten metal via CVD, achieving deposition in specified areas. During the deposition process, critical parameters such as temperature and pressure are controlled to enable rapid reduction of the tungsten precursor, thereby minimizing corrosion of the underlying material. This method avoids occupying the barrier layer in confined spaces, thereby reducing the contact resistance of the tungsten wire and further lowering the chip's power consumption. Additionally, it eliminates the need for CMP to remove excess tungsten in non-deposited areas, resulting in cost savings.

3.3. Atomic Layer Deposition

Atomic Layer Deposition, as a cutting-edge deposition method, forms thin films by alternately introducing gaseous reactants into a chamber where they adsorb onto the substrate surface and undergo chemical reactions. This pulsed alternating method enables the film to grow layer by layer at the atomic level, achieving precise control over the film's composition and other properties [11].

In the contact hole process, ALD is employed to deposit a thin TiN barrier layer, significantly reducing its spatial occupation and thereby lowering the contact resistance of tungsten. As shown in Fig.2, ALD of TiN involves four primary steps, with repeated cycles enabling layer-by-layer film growth [12].

First, the gas-phase titanium precursor $TiCl_4$ is introduced and adsorbed onto the substrate surface. Then, the unadsorbed gas-phase precursors and adsorbed reaction products are removed using an N_2/Ar inert gas purge. Next, the gas-phase nitrogen precursor NH_3 is introduced to react with Ti precursor molecules on the substrate surface, depositing a TiN film while simultaneously generating HCl gas as a byproduct. Finally, inert gas is introduced a second time to remove any unreacted gaseous precursors and reaction byproducts.

ALD grows thin films layer by layer at the atomic level, resulting in high-quality, dense films with strong barrier properties. Following subsequent cleaning, tungsten metal deposition is made on the surface [13].

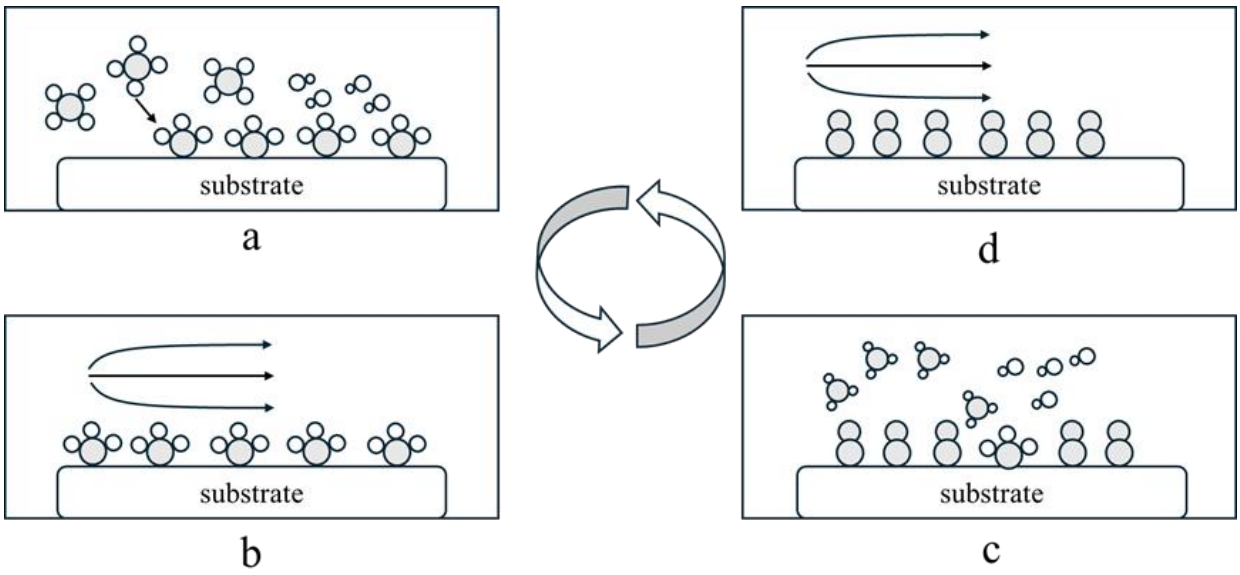


Fig 2. Main steps of ALD.

4. Comparative Analysis

The mainstream two-step Tungsten CVD technology and equipment are now relatively mature. The key challenge lies in enhancing step coverage capability by adjusting parameters such as temperature, pressure, gas flow rate, and gas ratio, thereby reducing the formation of voids and seams at high aspect ratios. Costs primarily come from the consumption of the tungsten precursor WF_6 and the treatment of the byproduct gas HF. The core of selective tungsten deposition lies in surface reaction control. Its selectivity demands higher standards for substrate surface and chamber cleanliness, requiring atomic-level precision control of the substrate surface (passivation, activation) [14]. The selection and dosage of inhibitors also necessitate continuous optimization through meticulous experimentation and simulation. The equipment complexity required for selective deposition far exceeds that of conventional tungsten CVD. While it reduces some costs associated with CMP, it demands greater investment in research and development as well as equipment. At present, machine learning modeling is applied to calculate parameters like pressure in area selective deposition, further enhancing the precision and efficiency of the process [15].

5. Analysis of Other Application Scenarios

5.1. Self-Aligned Gates

Precise alignment at the atomic level is one of the bottlenecks in nanodevice fabrication. Selective deposition differentially treats the substrate surface to ensure reactions occur only at desired locations. In the latest GAA technology, precise deposition of the metal gate is required to prevent leakage caused by errors. In traditional self-alignment processes, the polysilicon gate serves as the mask to achieve self-alignment of the source and drain. During selective deposition, the metal material can be deposited with self-alignment into the intended gate trenches. Dr. Li Yicheng's team innovatively enhanced the conventional two-step cyclic deposition process by controlling selective atomic layer deposition parameters and incorporating defect-specific treatment, thus achieving selective deposition without surface inhibitors. This study successfully achieved self-aligned patterning of tantalum oxide on copper/silicon dioxide substrates, effectively preventing unwanted nucleation defects within copper regions [16]. The self-alignment selectivity approached 100%, with no film growth observed in non-growth areas. This research presents a simplified and highly precise self-aligning manufacturing technique that significantly advances future device miniaturization.

5.2. Thin Film Encapsulation

Many devices, such as OLED displays and MEMS sensors, are highly sensitive to oxygen and water molecules in the air. The longer they are exposed, the more their performance gradually degrades until they eventually fail. Therefore, packaging is a key technology for protecting devices and extending their lifespan. Traditional packaging processes predominantly utilize rigid and heavy materials such as glass, which are unsuitable for modern lightweight, thin, and flexible electronic products. ALD can deposit dense films at the nanometer scale, whose ideal properties are well-suited for modern electronic packaging. However, due to its relatively low deposition rate, the industrial application of ALD is limited, necessitating the use of improved deposition methods to enhance the rate [17]. Chi-Hoon Lee's team explored the use of APCVD to fabricate high-performance Al_2O_3 films for OLED encapsulation at low temperatures (100°C). The film exhibits outstanding encapsulation performance with a WVTR of 4.4×10^{-5} g/(m^2 day) and achieves high productivity (37.44 Å/min) [18].

6. Conclusion

This paper reveals that, against the backdrop of continuous feature size scaling, the TiN barrier required for conventional tungsten CVD occupies an excessively high proportion within contact holes. This leads to increased contact resistance, impacting the power consumption of the device. Although ALD can produce high-quality ultra-thin barrier layers, its deposition rate is relatively slow and requires further process optimization. In contrast, selective deposition technology achieves region-specific growth without requiring a barrier layer, fundamentally resolving the issues associated with barrier layers. The significance of this research lies in establishing selective deposition as a key approach to overcoming the physical limits of contact resistance and enabling smaller feature sizes. Moving forward, selective deposition technology must be deeply integrated with innovative architectures such as novel two-dimensional channel materials (e.g., MoS_2). Accelerating its industrialization through AI-driven process optimization will ultimately provide core technological support for constructing high-performance, low-power next-generation integrated circuits.

References

[1] Xie C, Zhang Y, Zhang K, et al. Introduction of Gate-All-Around FET (GAAFET) [J]. Applied and Computational Engineering, 2023, 28(1): 164–175.

[2] Guo X, Zhao J, Qiao J, et al. Studies of Pecvd and Ozone CVD Deposition Rate, Uniformity and Step Coverage [J]. MRS Proceedings, 1994, 363.

[3] LI Jianzhi, LI Wenyuan, PAN Xu, et al. Effect of nitrogen flow rate on microstructure and properties of titanium nitride coatings[J]. Journal of Packaging Science, 2024, 16(5): 18-27, 51.

[4] YU Changmin, LUO Zhiyong, LIU Yu. Optimization of leakage current between source and drain in shielded gate trench MOSFETs[J]. Semiconductor Technology, 2023, 48(12): 1092-1096.

[5] XU S H, YAO P, ZHANG J D, et al. The filling seams improvement and properties analyses of tungsten films[J]. Microelectronic Engineering, 2020, 226: 111285.

[6] STEINHÖGL W, STEINLESBERGER G, PERRIN M, et al. Tungsten interconnects in the nano-scale regime[J]. Microelectronic Engineering, 2005, 82(3/4): 266-272.

[7] LI Fei. Investigation on step coverage and gap-fill capability of tungsten (W)[J]. Electronic Technology & Software Engineering, 2016, (10): 110-111.

[8] CHANG C Y, et al. Ultra-low (1.2×10^{-9} Ωcm2) p-Si0.55Ge0.45contact resistivity (ρc) using nanosecond laser anneal for 7nm nodes and beyond[C] // 2017 17th International Workshop on Junction Technology (IWJT). Uji, Japan: [s. n.], 2017: 23-26.

[9] Guo X, Zhao J, Qiao J, et al. Studies of Pecvd and Ozone CVD Deposition Rate, Uniformity and Step Coverage [J]. MRS Proceedings, 1994, 363.

[10] SUN J, YU Y, TANG J, et al. Plasma cleaning technology: Mechanisms, influencing factors, and applications[J]. IEEE Access, 2025, 13: 37221-37242.

[11] Riyanto E, Martides E, Junianto E, et al. The Growth Mechanisms of Atomic Layer Deposition: An Overview [J]. Eksergi, 2020, 17(2): 56.

[12] KIM S, AN H, OH S, et al. Atomistic kinetic Monte Carlo simulation on atomic layer deposition of TiN thin film[J]. Computational Materials Science, 2022, 213: 111620.

[13] YANG Xiaoliang. Research and application of surface cleaning and coating removal technology for titanium nitride coatings[J]. Cleaning World, 2025, 41(7): 10-12, 54.

[14] Young K T, Hsiao A, Brummer A, et al. Mechanisms of Area-Selective Atomic Layer Deposition and Their Impact on Feature Sizes [J]. The Journal of Physical Chemistry C, 2024, 128(35): 14790–14800.

[15] Tom M, Wang H, Ou F, et al. Machine Learning Modeling and Run-to-Run Control of an Area-Selective Atomic Layer Deposition Spatial Reactor [J]. Coatings, 2023, 14(1): 38.

[16] Li Y, Qi Z, Lan Y, et al. Self-aligned patterning of tantalum oxide on Cu/SiO_2 through redox-coupled inherently selective atomic layer Deposition [J]. Nature Communications, 2023, 14(1).

[17] Muñoz-Rojas D, Maindron T, Esteve A, et al. Speeding up the unique assets of atomic layer Deposition [J]. Materials Today Chemistry, 2019, 12: 96–120.

[18] Lee C-H, Yoo K S, Kim D, et al. Advanced Atmospheric-pressure spatial atomic layer deposition for OLED encapsulation: Controlling growth dynamics for superior film Performance [J]. Chemical Engineering Journal, 2025, 503: 158424.