# Designs of Low-Power Static Random-Access Memory

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**Abstract.** With the fast development of big data, Internet of Things (IoT), and edge computing, the memory systems are required to the highest ever, in which the performance and energy efficiency have significant impacts on the overall system capability. Three things about SRAM make it ideal for on-chip storage and cache memories, It features high read and write speeds, low dynamic power consumption for reading and writing, and a mature process. In this paper, we give an all-encompassing review of low-power SRAM design techniques, including circuit-level and architectural innovations along with the emerging Computing-In-Memory (CIM) paradigm. Techniques include novel circuit methodologies such as read/write-assist, as well as emerging transistor technologies like GAA nanosheets. This survey reviews techniques to reduce the dynamic and leakage power consumption, enhance writability and reliability in low-voltage operation, and minimize the energy overhead associated with data movement. This work systematically investigates conventional and emerging methods and offers insights into how to design energy-efficient SRAM for next-generation portable and AI-centric platforms.

**Keywords:** Low-power SRAM, write/read-assist, multi-port SRAM, GAA nanosheet, RibbonFET.

## 1. Introduction

The development of the big data era, coupled with the pervasive expansion of the Internet of Things (IoT), is fueling an unprecedented explosion in artificial intelligence, mobile computing, and wearable technologies. This paradigm shift has created an insatiable demand for data processing and storage, growing at an exponential rate. At the heart of this computational revolution, memory systems stand as a critical and defining component. Their performance, capacity, and—most critically—energy efficiency directly dictate the capabilities and battery durability of the entire system. As applications become increasingly data-centric, the role of memory has evolved from a passive storage element to a fundamental bottleneck and a primary determinant of overall system performance and power consumption.

There exists a wide variety of memory types. Among them, Static Random Access Memory (SRAM) is distinguished by its high-speed random-access capability and compatibility with logic process technologies, making it highly suitable for integration into register files and cache memories within System-on-Chips (SoCs). The density of SRAM arrays continues to increase with each successive process technology node, enabling greater on-chip storage capacity. However, this very scaling aggravates the leakage currents of MOS transistors, posing a fundamental challenge to power efficiency. This issue is particularly critical for battery-limited portable devices, where stringent power constraints are paramount. Consequently, designing low-power SRAM has become crucial.

In response to these pressing challenges, this research conducts a systematic investigation into design strategies for low-power SRAM. It focuses on conventional memory applications, analyzing key circuit-level and architectural approaches developed to mitigate power consumption, examining their operational principles, and evaluating their impact on both dynamic and static power. Additionally, this work extends its analysis to include relevant techniques in the context of computing-in-memory (CIM) architectures.

## 2. Preliminary

As shown in figure.1, basic 6T SRAM cell's operation centers around the cross-coupled inverters (M1-M4), which store a single bit as complementary voltages at nodes Q and QB. Access to this stored data is controlled by the WL (Word Line); when de-asserted (low), access transistors M5 and M6 are turned off, isolating the cell from the BL and BLB (Bit Line and complementary Bit Line). For a read operation, both BL and BLB are precharged high. Enabling the WL (high) allows the internal nodes to pull one bit line low through the corresponding drive transistor (M1 or M3), creating a measurable voltage difference. For a write operation, the desired data and its complement are driven onto the BL and BLB pair. Asserting the WL then enables these external signals to overpower the cross-coupled inverters via access transistors M5 and M6, forcibly flipping the states of Q and QB to store the new value.

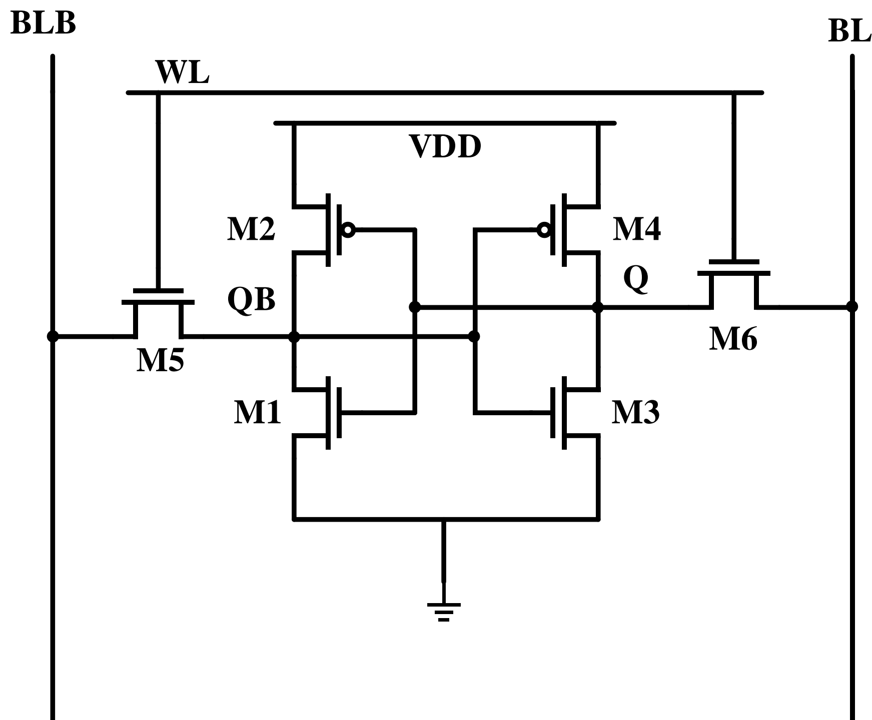



**Fig 1.** Schematic of 6T SRAM

## 3. Low-power SRAM designs

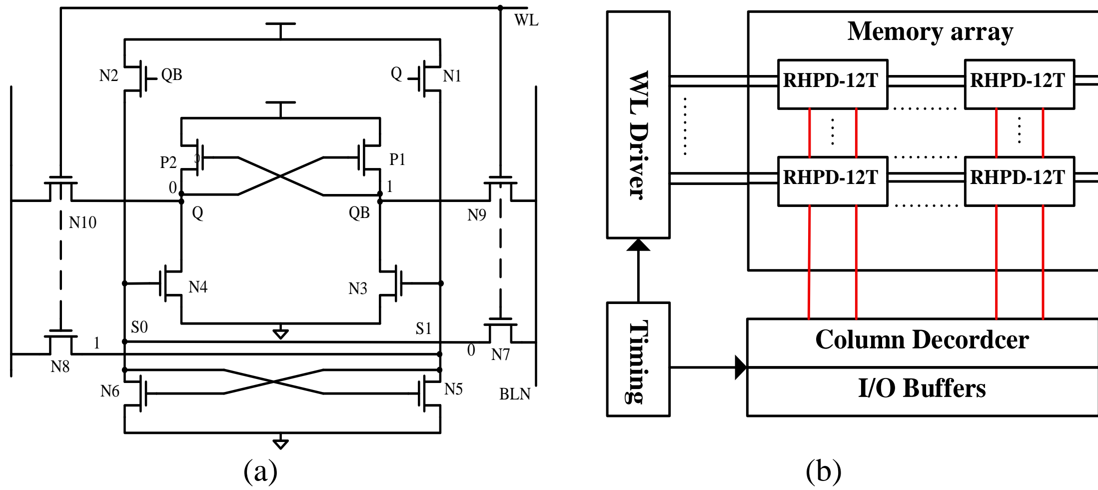
Low-power SRAM techniques primarily evolve around several key directions: advanced process nodes with superior electrostatic integrity, robust cell topologies and circuit assist techniques for low-voltage operation, architectural enhancements for efficient power and signal management, and computing-in-memory (CIM) schemes that reduce data transfer. The following cases exemplify these approaches.

In IEEE Transactions on VLSI Systems 2016, Aligarh Muslim University reported a single-ended Schmitt-Trigger-based robust low-power SRAM cell featuring an 11-transistor configuration comprising a cross-coupled Schmitt-Trigger (ST) inverter pair for robust data storage, a dedicated write-access transistor (MAL), a two-transistor read path (MAR1 and MAR2), and two feedback transistors (MNFL and MNFR) [1]. As shown in figure.2, this design employs a single-ended read/write structure, which significantly reduces dynamic power by halving the bitline (BL) switching activity compared to differential schemes. Additionally, during write operations, the disconnection of feedback transistor drains from Vdd further minimizes power dissipation.

**Fig 2.** Schematic of ST11T SRAM [1].

In a 2022 IEEE International Electron Devices Meeting (IEDM) paper, Global TCAD Solutions proposed a low-power SRAM design using Gate-All-Around Nanosheet (GAA NSH) transistors at the 3nm technology node [2]. Their method focused on minimizing the minimum operating voltage (Vmin) through the NSH structure's superior short-channel control. This allowed for the use of lower channel doping, which directly reduced variability from Random Discrete Dopants (RDD) and was a key factor in achieving a Vmin improvement of up to 28mV compared to FinFETs. Furthermore, they utilized the unique design freedom of NSH for non-digital n/pFET width balancing and optimized the vertical sheet pitch (VSP). This co-optimization of device and design parameters, performed through a variability-aware DTCO flow, enabled them to simultaneously improve read delay (td, read) by 21% and reduce cell area by 14% while maintaining a lower Vmin, thus demonstrating a path for significant power reduction in advanced SRAM cells.

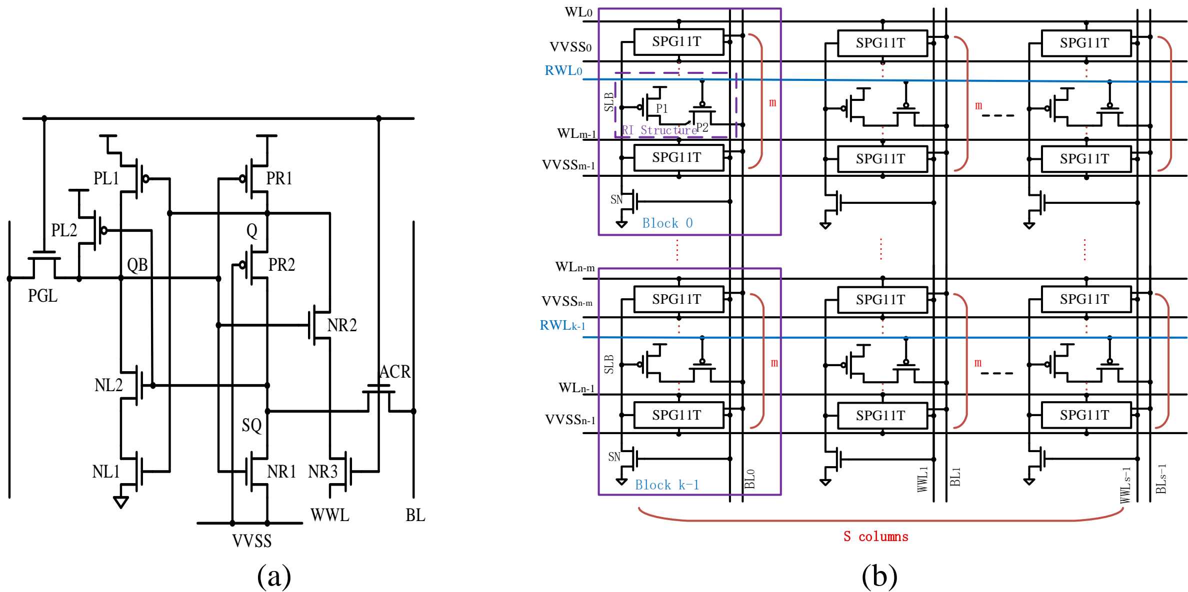
In IEEE Transactions on VLSI Systems 2020, National Tsing Hua University reported a novel write-enhanced and highly reliable RHPD-12T SRAM cell for space applications that achieves low power consumption through an ingenious circuit and array architecture, as detailed in Fig. 3(a) and (b) [3]. The core innovation lies in the cell's polarity design shown in Fig. 3(a), which employs 10 nMOS and only 2 pMOS transistors to leverage the inherently lower leakage current of nMOS, thereby significantly reducing static power. Moreover, the four-transistor (N7-N10) parallel write path enables simultaneous data application to internal nodes during write operations, accelerating write speed and reducing dynamic power by shortening the activation time of high-capacitance nodes. The array-level architecture in Fig. 3(b) illustrates how these cells are efficiently integrated, sharing wordline and bitline resources to minimize peripheral circuit overhead and further enhance overall system-level power efficiency. This robust parallel-write mechanism also ensures a high write success rate under harsh conditions such as low supply voltage and high frequency, avoiding additional power overhead from write retries. Consequently, through a co-design approach spanning from transistor selection and cell topology to array organization, the RHPD-12T achieves excellent energy efficiency while maintaining high reliability.



(a) (b)

**Fig 3.** (a) Proposed RHPD-12T memory cell. (b) Structure of SRAM cell with RHPD-12T cell array [3].

In IEEE Transactions on VLSI Systems 2019, Anhui University reported a half-select disturb-free 11T SRAM cell with a built-in write/read-assist scheme that achieves ultralow-power operation by enabling reliable functionality at a minimum supply voltage of 0.435 V through two key techniques [4]. First, a built-in write/read-assist scheme enhances stability at low voltages. Transistor PR2 (Fig. 4(a)) provides dynamic node isolation during write operations to improve write margin, while a Read-Improvement structure (Fig. 4(b)) maintains bitline voltage during read operations to ensure read stability. Second, the cell's inherent immunity to half-select disturbs enables a power-efficient bit-interleaving architecture. The design isolates storage nodes in half-selected cells, eliminating disturbance issues without additional power overhead. This disturbance-free characteristic allows implementation of bit-interleaving for enhanced soft-error immunity while maintaining low power consumption. By combining these approaches, the cell achieves a significant reduction in both dynamic and leakage power, making it suitable for ultralow-voltage applications. The integrated assist scheme and disturbance-free operation work synergistically to push the operational voltage limit while maintaining reliability.



(a) (b)

**Fig 4.** (a) The SPG11T SRAM cell. (b) n × s SPG11T SRAM array [4].

In the IEEE Journal of Solid-State Circuits 2021, University of Electronic Science and Technology of China reported a two-direction in-memory computing based on 10T SRAM with horizontal and vertical decoupled read ports that present a highly symmetric and reconfigurable 10T SRAM architecture, which achieves low-power operation by enabling flexible in-situ data processing without

costly data movement [5]. The cell features horizontally and vertically decoupled read ports, controlled by independent word lines (RWL and CWL), as shown in Fig. 5. This symmetric design allows the memory array to be accessed and activated in both row and column directions, supporting native in-memory logic operations—such as AND and OR—across multiple rows or columns without transposing data layout. The same structure also facilitates efficient matrix transposition and bidirectional content-addressable memory (CAM) search, leveraging the reconfigurable use of bit lines and read lines as either search lines or match lines.

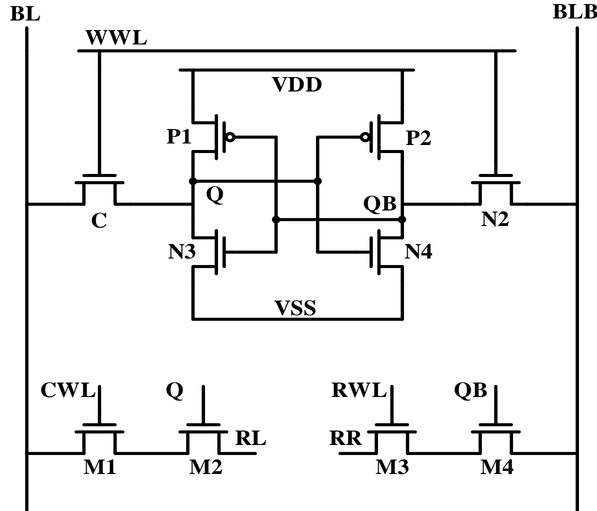



**Fig 5.** Schematic of the 10T cell [5].

Additionally, a self-termination circuit (Fig.6) further reduces energy consumption by dynamically cutting off the discharge path upon detecting a match, minimizing unnecessary switching activity. By integrating bidirectional access, in-memory computing, and energy-aware operation into a unified architecture, the design significantly reduces the energy overhead associated with data transfer and parallel processing.

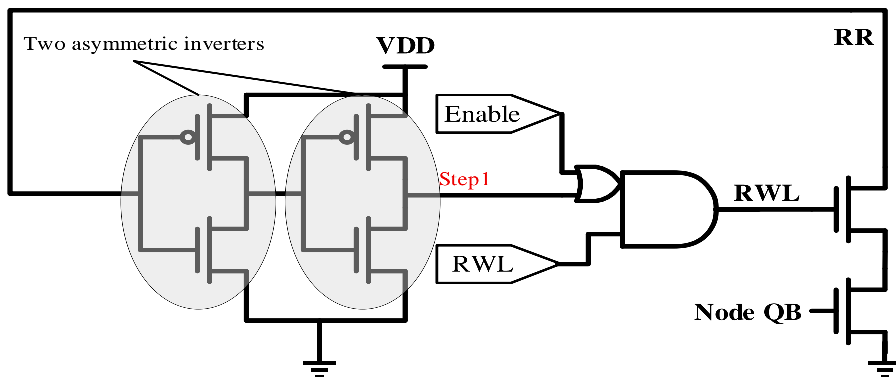
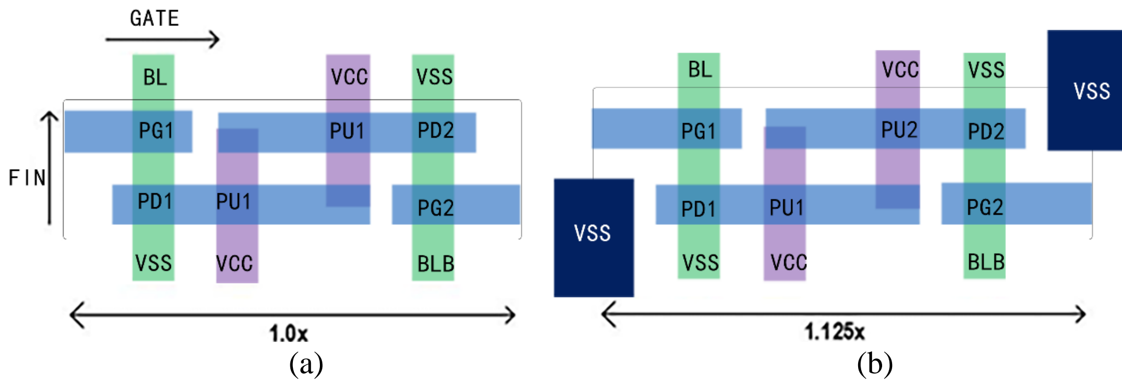



**Fig 6.** Schematic of self-termination structure [5].

In ISSCC 2020, X. Si et al. reported a 28nm 64Kb 6T SRAM computing-in-memory macro that achieves ultra-low power consumption by embedding multiply-and-accumulate operations directly within the memory array [6]. This architecture eliminates energy-intensive data movement by processing data where it is stored, dedicating nearly all power consumption to productive computation rather than data transport, thereby achieving orders-of-magnitude improvement in energy efficiency for AI edge chips.

Intel Corporation reported in IEEE Solid-State Circuits Letters (2024) a 2048×60m4 SRAM in Intel 4 that uses an around-the-array power delivery scheme based on PowerVia [7]. Instead of integrating PowerVias directly into the bitcell, which would cause area overhead, the scheme places PowerVias around the array boundary, thereby reducing IR drop while keeping the cell compact. The comparative layouts of the HDC bitcell with and without PowerVia implementation can be seen in

Fig. 7. This configuration improves the effectiveness of wordline-underdrive circuits at low voltage and enhances read stability, while at the same time lowering dynamic energy consumption by accelerating bitline pre-charge and VCC restoration. In addition, peripheral compaction techniques, including tap removal and standard-cell height reduction, further decrease macro area and contribute to energy-efficient operation.




(a) (b)

**Fig 7.** HDC bitcell layout (a) without PowerVia and (b) with PowerVia for VSS [7].

Synopsys reported in ISSCC 2025 a 38Mb/mm² dual-rail SRAM fabricated in 3nm FinFET technology, which introduces an interface dual-rail (IDR) architecture that decouples the array supply voltage from the external interface voltage [8]. This design enables SRAM functionality to operate normally at 380 mV, which is a low interface voltage, while it maintains stability and density. To improve energy efficiency, the authors proposed a wide-range level shifter with an integrated latch, which can mitigate contention and reduce delay and power consumption during voltage conversion. In addition, by gating the internal VDDA power domain during standby, leakage can be significantly reduced without affecting data retention, making this design particularly suitable for aggressive SoC voltage scaling.

TSMC reported in ISSCC 2024 a 3nm FinFET pseudo-2-port SRAM that achieves 21.1Mb/mm² density and operates at 4.3 GHz through a double-pumping scheme supporting one read and one write per cycle [9]. To maintain both high speed and low power, the design incorporates a folded-bitline multi-bank architecture that improves array density and reduces parasitic loading. Several innovative circuits are employed: a sense-amplifier enables interlock, minimizes the read window, and suppresses unnecessary transitions, a WL-negating shortcut-control generator with real-time dynamic performance scaling adapts timing dynamically for energy and performance balance, and a pre-loading write driver reduces write energy by overlapping pre-charge with normal operations. The proposed WL-negating shortcut (WLNS) structure is illustrated in Fig. 8. Together, these optimizations allow the SRAM to sustain low-voltage operation while delivering multi-port functionality with high efficiency.

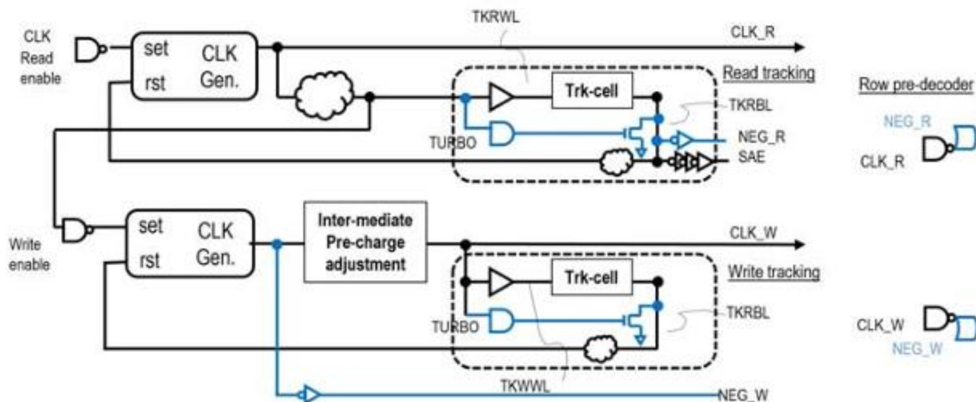



**Fig 8.** Proposed WL negating shortcut (WLNS) [9].

Intel reported in ISSCC 2025 a 0.021 μm² high-density low-power SRAM implemented in Intel-18A technology using RibbonFET transistors and PowerVia backside power delivery [10]. Combined innovations at the device and circuit levels effectively enable energy-efficient SRAM operation with record-high density in advanced process nodes. The backside power delivery network significantly reduces IR drop and improves power efficiency by minimizing voltage loss and routing congestion. Furthermore, a negative bitline (NBL) write-assist scheme, realized through backside metal capacitors beneath the array, generates the required negative voltage without additional area, thereby enhancing writability and reducing the minimum operating voltage (Vmin) by 68 mV. In addition, the RibbonFET architecture allows continuous transistor width tuning to optimize pass-gate to pull-down ratios, improving both read and write margins without resorting to conventional assist circuits.

Yonsei University and Articron reported in ISSCC 2024 a novel self-enabled write-assist cell architecture designed for high-density SRAM operating in resistance-dominated sub-5nm technology nodes [11]. In such cases, the increased interconnect resistance can significantly reduce writability, but the SEWAC scheme improves write performance by directly introducing additional write paths between in-place cells. These paths are automatically triggered during write operations without the need for extra timing signals or dummy cells. Compared with traditional auxiliary schemes, SEWAC can achieve higher writability yield, occupies minimal area overhead, and can tolerate bitline resistances of up to 240 Ω.

TSMC reported in ISSCC 2024 a low-power 3nm dual-port SRAM [12]. The optimized backend interconnect structure minimizes parasitic resistance and capacitance, effectively reducing RC delay and dynamic power during both read and write operations. To further enhance writability at low supply voltages, the proposed far-end write-assist scheme dynamically compensates for voltage drops along long bitlines, maintaining stable cell access and reducing the minimum operating voltage (0.7V) without additional energy overhead. Together, these techniques enable high-frequency (3.6 GHz) dual-port operation with significantly lower power consumption and improved stability. A simplified schematic of the SRAM bitcell with the P/G strap connection is shown in Fig. 9.

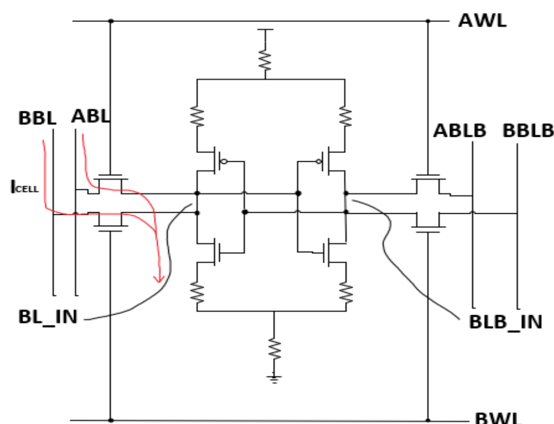



**Fig 9.** Simplified SRAM bitcell schematic with P/G strap connection [12].

## 4. Conclusion

This study has systematically examined the landscape of low-power SRAM design, highlighting key innovations across circuit topologies, process technologies, and architectural strategies. This paper mainly studies the bitcell design based on advanced CMOS technology, the low-power strategy of SRAM, and in-memory computing. These methods address the key challenges of reducing leakage, voltage scaling, and data movement overhead. While emerging computing-in-memory schemes show great promise, traditional pure-memory SRAM cells continue to be essential for high-density storage applications and remain an important research direction for future memory systems. As technology

nodes continue to advance, the co-optimization of devices, circuits, and architectures will remain essential to achieving the energy efficiency required by next-generation intelligent and edge systems.

## Authors Contribution

All the authors contributed equally, and their names were listed in alphabetical order.

## References


[1] Ahmad S, Gupta MK, Alam N, Hasan M. Single-Ended Schmitt-Trigger-Based Robust Low-Power SRAM Cell. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24(8): 2634-2642.

[2] Rzepa G, et al. Performance and Variability-Aware SRAM Design for Gate-All-Around Nanosheets and Benchmark with FinFETs at 3nm Technology Node. 2022 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2022: 15.1.1-15.1.4.

[3] Zhao Q, Peng C, Chen J, Lin Z, Wu X. Novel Write-Enhanced and Highly Reliable RHPD-12T SRAM Cells for Space Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28(3): 848-852..

[4] He Y, Zhang J, Wu X, Si X, Zhen S, Zhang B. A Half-Select Disturb-Free 11T SRAM Cell With Built-In Write/Read-Assist Scheme for Ultralow-Voltage Operations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27(10): 2344-2353.

[5] Lin Z. Two-Direction In-Memory Computing Based on 10T SRAM With Horizontal and Vertical Decoupled Read Ports. IEEE Journal of Solid-State Circuits, 2021, 56(9): 2832-2844.

[6] Si CX. A 28nm 64Kb 6T SRAM Computing-in-Memory Macro with 8b MAC Operation for AI Edge Chips. 2020 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2020: 246-248Kim D, et al. A 2048×60m4 SRAM Design in Intel 4 With Around-the-Array Power Delivery Scheme Using PowerVia. IEEE Solid-State Circuits Letters, 2024, 7: 243-246.

[7] Ilo H. A 38Mb/mm2 380/540mV Dual-Rail SRAM in 3nm-FinFET Technology. 2025 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2025: 498-500.

[8] Haraguchi M. A 3nm FinFET 4.3GHz 21.1Mb/mm2 Double-Pumping 1-Read and 1-Write Pseudo-2-Port SRAM with Folded-Bitline Multi-Bank Architecture. 2024 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024: 280-282.

[9] Wang X. A 0.021μm2 High-Density SRAM in Intel-18A-RibbonFET Technology with PowerVia-Backside Power Delivery. 2025 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2025: 494-496.

[10] Yeo M. Self-Enabled Write-Assist Cells for High-Density SRAM in a Resistance-Dominated Technology Node. 2024 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024: 282-284.

[11] Fujiwara H. A 3nm 3.6GHz Dual-Port SRAM with Backend-RC Optimization and a Far-End Write-Assist Scheme. 2025 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2025: 500-502.