# Research Progress on CMOS Leakage Current Optimization and Low-Power Design

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**Abstract.** With the continuous scaling of semiconductor technology into the nanometer regime, leakage current in CMOS integrated circuits has become a major bottleneck limiting low-power design and performance improvement. This paper focuses on the leakage current optimization, systematically analyzing representative low-power techniques from both device and circuit perspectives. At the device level, a combined low-temperature annealing and oxidation process is employed to effectively suppress carbon vacancy defects, thereby reducing the reverse leakage current in 4H-SiC diodes. At the circuit level, the Input Vector Analysis and Transistor Stacking (IVATS) technique minimizes standby current through the stacking effect, while the feedback structure low-power adder improves computational delay along with leakage reduction. The results show that all three approaches achieve significant leakage suppression; however, they still face limitations in terms of applicability, design complexity, and process scalability. To address these issues, this work provides a critical assessment and proposes corresponding improvement directions, including process parameter optimization, enhanced design automation, and cross-layer co-optimization. It is concluded that the integration of device-level process improvements with circuit-level architectural optimization is a key pathway toward achieving high performance and low power consumption in advanced CMOS technology nodes.

**Keywords:** CMOS Integrated Circuits; Leakage Current Optimization; 4H-SiC Diodes; Input Vector Analysis; Feedback Structure.

## 1. Introduction

With the rapid development of information technology and manufacturing industries, CMOS integrated circuits have become the core foundation of modern electronic systems. Driven by Moore’s Law, semiconductor technology has continued to scale down, entering the nanometer era, which has significantly improved the performance, power efficiency, and integration density of CMOS circuits. The total power consumption of CMOS circuits mainly consists of dynamic and static components. At technology nodes above 100 nm, dynamic power dominates; however, as scaling advances below 100 nm, static power-particularly leakage power-has become a key factor limiting circuit performance and energy efficiency [1]. In the current sub-20 nm technology environment, leakage current has become a major bottleneck for low-power design. Therefore, research on leakage current optimization techniques in CMOS integrated circuits holds great theoretical and engineering significance.

Leakage current primarily originates from three sources: 1. reverse-biased PN junction leakage due to heavily doped drain and source regions; 2. subthreshold leakage through the channel of an off-state transistor; and 3. gate tunnelling current caused by the extremely thin gate oxide layer [2]. Studies have shown that gate leakage increases exponentially as oxide thickness decreases, making it a significant contributor to total power consumption in nanometer-scale CMOS processes [3].

To address leakage issues, researchers have proposed various optimization techniques at both device and circuit levels. At the device level, common approaches include adopting metal gate electrodes, introducing high-k dielectric materials, and optimizing doping profiles to suppress subthreshold and gate leakage currents [4]. At the circuit level, techniques such as multi-threshold design, transistor stacking, and standby leakage control have been widely used. Representative schemes include Multi-Threshold CMOS (MTCMOS), Dual-Threshold CMOS, Variable-Threshold

CMOS (VTCMOS), and Dynamic-Threshold CMOS [5]. These methods have proven effective in reducing static power consumption and have been widely applied in practical chip design.

However, existing studies still face several challenges. Device-level improvements in materials and structures, while effective, often increase process complexity and manufacturing costs; circuit-level techniques, on the other hand, tend to trade off speed or area for lower power, making it difficult to balance performance and efficiency. Moreover, as technology nodes continue to scale down, the applicability and scalability of traditional methods are becoming increasingly constrained.

This paper aims to systematically review the mechanisms and types of CMOS leakage current, summarize current design techniques and research progress, and analyze representative achievements from both device and circuit perspectives. Furthermore, it discusses existing limitations and challenges, and proposes potential development directions and optimization strategies. The study not only deepens the understanding of low-power CMOS circuit design but also provides valuable insights for future high-performance and energy-efficient system optimization.

## 2. Models and Methodologies

To systematically present recent progress in leakage current optimization and low-power design, this study reviews representative research models from different levels. In general, related studies can be classified into two main categories. The first category focuses on device-level process and structural improvements, which aim to suppress subthreshold and gate leakage currents by optimizing gate dielectric materials or adopting advanced fabrication techniques. For instance, employing high-k dielectric materials such as Tantalum Pentoxide ($Ta_2O_5$) as the MOSFET gate dielectric can achieve lower power consumption under the same gate bias [6]. The second category emphasizes circuit-level design and architectural optimization, where techniques such as MTCMOS, VTCMOS, power gating, and transistor stacking are employed to reduce standby power. These methods have been extensively studied and widely applied in modern low-power chip design [7]. This paper further analyzes several representative models, as shown in Fig. 1, summarizing their technical principles and experimental results, thereby providing a theoretical basis for the subsequent discussion on limitations and potential improvements.

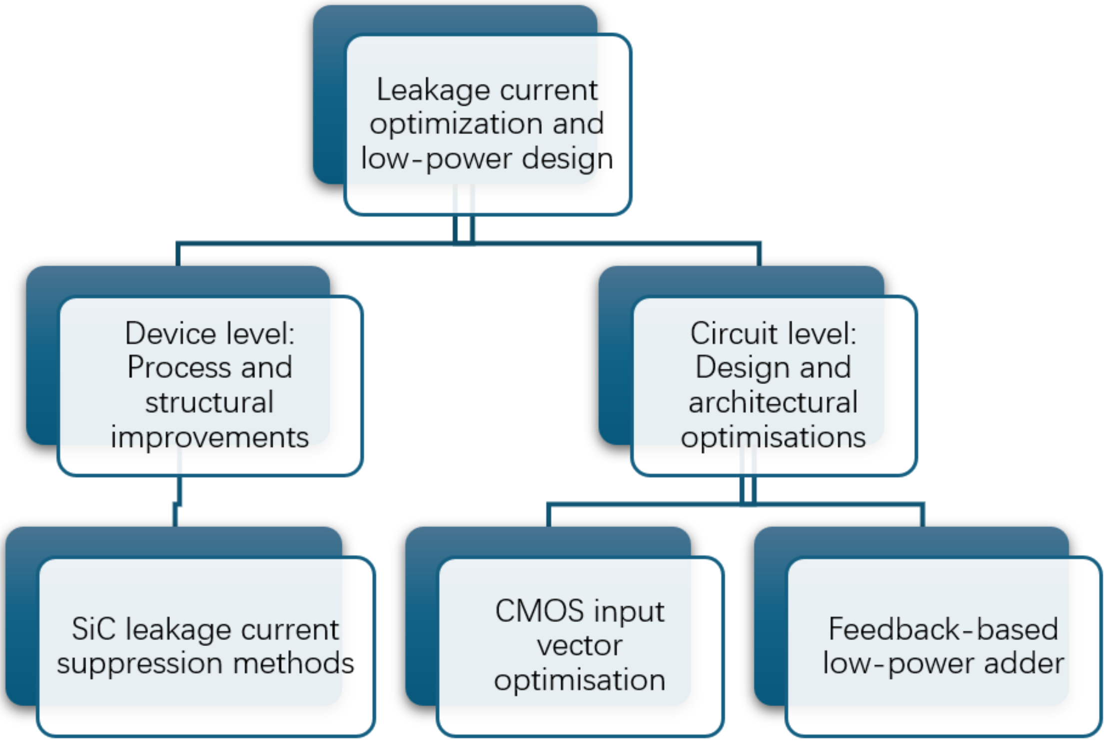

**Fig. 1** Research framework of leakage current optimization and low-power design

### 2.1. Techniques for Suppressing Leakage Current in SiC-Based Devices

At the device level, Lin et al. proposed a novel process combining low-temperature annealing and oxidation for 4H-SiC power diodes to effectively suppress reverse leakage current [8]. While conventional high-temperature annealing can fully activate aluminium dopant atoms, it simultaneously introduces a large number of carbon vacancy defects. These vacancies act as additional current pathways under reverse bias, significantly increasing leakage current. To address this issue, the researchers employed a lower annealing temperature to slow down the generation rate of carbon vacancies. Subsequently, carbon interstitials were introduced during oxidation, which combined with the vacancies to achieve defect passivation. Experimental results demonstrated that, compared with conventional processes, this approach reduced reverse leakage current by approximately 32 times under -1200 V operation, while also increasing the barrier height and improving rectification characteristics. Further analysis revealed a direct correlation between the reduction of leakage current and the significant decrease in carbon vacancy defects. This case exemplifies an effective strategy for leakage current suppression through process optimisation and defect engineering, providing valuable insights for enhancing the performance and reliability of high-voltage SiC power devices.

### 2.2. Input Vector Control Techniques for CMOS Leakage Reduction

At the circuit level, Zhang et al. proposed an input-vector and transistor-stacking-based leakage suppression technique (IVATS) to address the limited effectiveness of traditional methods in low-power applications [9]. The approach analyses the input combinations of circuits in standby mode to determine the optimal input vector and selectively introduces stacked transistors in critical paths, thereby exploiting the stacking effect to reduce subthreshold leakage current. Compared with full-stacking or high-threshold device techniques, IVATS can more precisely identify dominant leakage paths, avoiding unnecessary area overhead and delay penalties. Experimental results showed that, in a 28 nm tri-state latch, the proposed method achieved an average leakage power reduction of approximately 42%, maintaining a 26.9% improvement even after place-and-route. Furthermore, in an FFT module, system-level leakage was reduced by around 17.5%. The study demonstrates that IVATS applies not only to cell-level circuits but can also be extended to IoT and low-frequency systems, offering a novel approach for low-power optimisation in near-threshold CMOS circuit design.

### 2.3. A Feedback-Controlled Low-Power Adder Circuit Architecture

Building on existing circuit-level leakage reduction research, Rani et al. introduced a feedback-controlled low-power technique that achieves simultaneous reductions in leakage current and propagation delay under 22 nm CMOS technology [10]. Unlike earlier approaches such as sleep transistors or LECTOR, which often suffer from unstable output levels and increased delay, this method integrates a high-threshold NMOS transistor within the pull-down network and incorporates an inverter-based feedback loop. During input transitions, the feedback circuit rapidly deactivates the NMOS device, effectively cutting off redundant current paths, minimising transient currents, and stabilising output voltage levels. Experimental results demonstrated that the leakage current of a NOT gate decreased from 393 nA to 1.94 nA, while the propagation delay was reduced from 4.6 ms to 0.24 ms. Significant improvements were also observed in NAND and full adder circuits. Although it introduces a minor area overhead, this feedback-driven architecture successfully balances low-power operation and high-speed performance, offering a practical and efficient solution for modern VLSI circuit design.

## 3. Limitations and Challenges

In addition to the research models discussed in Section 2, numerous leakage optimisation and low-power design techniques have been proposed in recent years. However, these studies still exhibit several limitations. On one hand, many approaches rely heavily on specific fabrication processes or application scenarios, resulting in limited generality and scalability. On the other hand, while some methods effectively reduce power consumption, they often incur higher design costs and increased circuit complexity, thereby diminishing their practicality. Moreover, a significant portion of current research remains confined to basic cells or small-scale circuit validations, lacking investigation into their adaptability to large-scale systems and advanced technology nodes. Therefore, it is necessary to conduct an in-depth analysis and evaluation of the representative studies summarised in Section 2, in order to identify their deficiencies and challenges, and to provide theoretical support for subsequent improvements and future research directions.

### 3.1. Limitations of Device-Level Techniques

Although the work by Jin et al. provided an effective approach for suppressing carbon vacancy defects and reducing the reverse leakage current of 4H-SiC JBS diodes [8], several limitations still remain. Firstly, while low-temperature annealing successfully inhibits the formation of carbon vacancies, it inevitably reduces dopant activation efficiency. This trade-off implies that achieving lower leakage current may come at the cost of degraded on-state conductivity. Unless an improved balance between defect suppression and dopant activation can be established in the future, the applicability of this process will remain limited. Secondly, the study focuses exclusively on JBS diodes, which feature relatively simple device structures. In more complex power devices such as MOSFETs or IGBTs, leakage mechanisms are not confined to carbon vacancies but may also involve channel-related defects and interface traps. Hence, directly extending this process to other devices introduces significant uncertainty. Moreover, although the authors used DLTS analysis and the Poole–Frenkel emission mechanism to verify the correlation between reduced carbon vacancies and lower leakage current, the quantitative relationship between oxidation parameters (e.g., temperature and duration) and defect recombination efficiency remains unclear. This raises concerns regarding the reproducibility and industrial stability of the process. Furthermore, the proposed method remains at the experimental verification stage and lacks long-term reliability testing or large-scale production validation. Without a unified mechanism that can be generalised across devices and fabrication processes, this approach may struggle to support the widespread deployment of high-voltage SiC power devices.

### 3.2. Applicability and Challenges of Input Vector Optimisation

The IVATS technique, which combines input vector analysis with transistor stacking, has demonstrated significant effectiveness in reducing leakage current in CMOS circuits. However, its applicability still faces several limitations [9]. Firstly, the method relies on input probability modelling and port leakage characterisation, which increase design complexity and impose stricter requirements on EDA tool capabilities, potentially becoming a bottleneck in large-scale circuit implementations. Secondly, although the technique performs well under the 28 nm EHVT process, its optimisation strategy may become ineffective as device architectures evolve toward FinFET and GAAFET technologies, where leakage mechanisms differ substantially. Furthermore, current research mainly targets low-frequency, always-on modules such as storage cells and FFT blocks, with insufficient evaluation on high-speed and dynamic logic circuits. Without balancing delay and power consumption, its general applicability remains limited. In addition, the physical boundary of the stacking effect constrains scalability—when stacking depth exceeds two transistors, gate leakage tends to offset the reduction in subthreshold current, while the weaker stacking effect in PMOS devices further restricts circuit topology and stacking configuration. Lastly, the analysis was conducted under typical process corners (TT/25 °C) and assumed uniform input distributions, which fail to capture complex real-world operating conditions. Unless a standardised optimisation framework applicable across processes and scenarios is established in future work, the scalability and practical adoption of IVATS will remain constrained.

### 3.3. Limitations of Feedback-Based Adder Design

The CMOS adder based on a feedback-controlled structure demonstrates excellent leakage suppression and delay reduction under 22 nm technology, showing clear advantages over conventional schemes such as LECTOR and sleep transistors [10]. However, several limitations remain. Firstly, the introduction of additional feedback paths and high-threshold transistors increases both circuit area and design complexity. This could become a critical constraint in area-sensitive or high-density designs and may indirectly raise dynamic power consumption due to more complex interconnections. Secondly, the experimental validation of this method was limited to basic logic gates (NOT, NAND) and a one-bit full adder. Although the reported improvements are notable, the absence of tests on multi-bit arithmetic units, pipelined structures, or system-level circuits restricts its scalability and generalisation. Moreover, the study primarily focuses on static leakage reduction, with insufficient discussion of dynamic power, signal integrity, and noise tolerance. Under high-frequency conditions, the feedback path may introduce additional switching energy or timing uncertainty, potentially degrading overall energy efficiency and stability. Finally, since the method was developed using 22 nm CMOS technology, its adaptability to emerging process nodes such as FinFETs and GAAFETs remains unverified, where device behaviour and leakage mechanisms differ substantially. Overall, while the technique exhibits strong performance in small-scale circuits, broader adoption will require further optimisation in area efficiency, dynamic power management, and cross-technology compatibility.

## 4. Recommendations and Proposed Solutions

As discussed in the preceding sections, recent research on leakage current suppression and low-power design has evolved from single-method approaches toward multi-level collaborative optimisation, encompassing both defect engineering at the device level and architectural optimisation at the circuit level. Although these techniques have achieved notable progress in reducing static power consumption, the fundamental trade-off between power efficiency and performance at advanced technology nodes remains unresolved. With the continuous downscaling of CMOS processes and the industrial adoption of emerging materials such as SiC, conventional optimisation strategies face increasing challenges, including limited adaptability, restricted validation scope, and rising design complexity. Based on the foregoing analysis, this study proposes targeted recommendations and potential improvement strategies for three representative research models across both device and circuit domains. These suggestions aim to enhance the adaptability and sustainability of low-power design methodologies in future FinFET, GAAFET, and large-scale integrated system technologies.

### 4.1. Recommendations for Device-Level Leakage Optimisation

For the combined low-temperature annealing and oxidation process, future research should focus on further optimisation of the process window to achieve a balance between defect suppression and dopant activation. One potential direction is to employ a multi-stage or multi-zone annealing strategy, supported by process simulation and mathematical modelling, to quantitatively evaluate the recombination efficiency between carbon interstitials and carbon vacancies, thereby enhancing process controllability. In addition, the proposed method should be extended to more complex power devices such as MOSFETs and IGBTs to validate its universality and effectiveness across different device architectures.

At the industrial level, large-scale experiments and long-term reliability tests—such as high-temperature and bias-stress evaluations—are necessary to ensure its robustness under extreme operating conditions like high voltage and high temperature. Furthermore, future studies could explore the integration of this defect-engineering approach with other process innovations, such as the incorporation of advanced gate dielectrics, to form a systematic process improvement framework. Such integration could further promote the widespread adoption of SiC technology in high-voltage and high-temperature applications.

### 4.2. Recommendations for Expanding and Improving Input Vector Optimisation Techniques

The IVATS technique demonstrates the feasibility of reducing circuit-level leakage through input vector analysis and transistor stacking. However, future development should focus on enhancing its generality and portability across different technologies and applications. One promising direction is the integration of machine learning algorithms or automated design tools to reduce design complexity and shorten the development cycle. Additionally, combining IVATS with traditional approaches such as MTCMOS could lead to a hybrid low-power design framework that remains effective under higher-frequency and more complex operating conditions.

For advanced technology nodes, it is recommended to redesign and re-evaluate IVATS within FinFET and GAAFET architectures to verify its adaptability to new leakage mechanisms and 3D device structures. System-level validation is also essential—for instance, applying the technique to arithmetic logic units (ALUs) or memory arrays—to assess its balance between performance and energy efficiency in large-scale circuits. Future research should particularly focus on ensuring method stability across various design scales and process conditions, thereby establishing IVATS as a truly general and reusable tool for modern low-power circuit design.

### 4.3. Optimisation Strategies and Application Prospects for Feedback-Based Adders

Experimental results at the 22nm CMOS technology node demonstrate that feedback-based structures outperform existing methods in reducing leakage current and propagation delay. However, challenges remain regarding scalability and adaptability to future process technologies. The application scope of this approach can be extended to multi-bit adders, multipliers, and arithmetic logic units (ALUs) to evaluate its effectiveness in more complex arithmetic circuits. Meanwhile, a modular feedback design strategy could be explored to minimise area overhead while improving circuit integration density.

From a power perspective, future studies should go beyond static leakage analysis and include dynamic power, signal integrity, and system reliability as key evaluation metrics to ensure consistent performance under high-frequency operation. For advanced technology nodes, it is recommended to redesign the feedback logic based on the specific electrical characteristics of FinFET or GAAFET devices to maintain both efficiency and stability. If an improved balance between design complexity and energy efficiency can be achieved, this technique has the potential to evolve into a versatile logic architecture for high-speed, low-power arithmetic circuits.

To provide a clearer comparison of the discussed approaches, Table 1 summarises the key limitations and corresponding improvement strategies for the three representative leakage optimisation models analysed in this study. This comparative overview highlights both the technical challenges and potential research directions at the device and circuit levels, serving as a concise reference for future optimisation of CMOS low-power design.

**Table 1.** Limitations and Recommended Improvements of Typical Leakage Optimisation Models

| Research Model | Limitations and Challenges | Recommendations and Improvement Measures |
|---|---|---|
| SiC Leakage Suppression Method | Low-temperature annealing may reduce conduction capability; verification is limited to JBS diodes with poor generality, lack of long-term stability and large-scale process validation. | Optimise the process window to improve controllability; extend the method to complex devices such as MOSFETs; conduct long-term and large-scale reliability tests. |
| CMOS Input Vector Optimisation (IVATS) | High design complexity due to dependence on input modelling and layout adjustments; validation limited to low-frequency storage and FFT modules; constrained by stacking depth and device-type variations | Introduce machine learning or automation to reduce design complexity; combine with traditional techniques such as multi-threshold CMOS to broaden applicability; extend to FinFET/GAAFET processes and large-scale circuit verification. |
| Feedback-Based Low-Power Adder | Additional transistors and feedback paths increase area and circuit complexity; validation is limited to basic logic gates and 1-bit adders; lacks evaluation of dynamic power and process adaptability. | Validate in multi-bit adders and complex logic structures; optimise layout to reduce area overhead; analyse dynamic power and performance in advanced technology nodes and high-frequency applications. |

## 5. Summary

This paper presents a systematic study on leakage current suppression and low-power design in CMOS integrated circuits, analysing and comparing three representative models from both the device and circuit perspectives. The results show that, at the device level, the combination of low-temperature annealing and oxidation effectively reduces the reverse leakage current in SiC diodes. At the circuit level, the input vector optimisation technique significantly lowers standby power consumption under low-frequency operation, while the feedback-based low-power adder achieves reduced propagation delay without sacrificing power efficiency.

Overall, these studies provide valuable insights into multi-level and multi-path approaches for leakage optimisation. This work highlights not only the limitations of existing methods in terms of process window, applicability, and design complexity but also the necessity of achieving cross-level cooperative optimisation. It is concluded that only by integrating material-level improvements, circuit-level design optimisation, and system-level energy efficiency control can a balance between power consumption and performance be maintained in advanced technology nodes. Future research should focus on enhancing automation, intelligence, and scalability, thereby promoting the broader application of low-power technologies and providing both theoretical and practical references for next-generation high-performance electronic systems.

## References

[1] Sharma V K. A survey of leakage reduction techniques in CMOS digital circuits for nanoscale regime. Australian Journal of Electrical and Electronics Engineering, 18(4): 217–236, 2021.

[2] Hemantha S, Dhawan A and Kar H. Multi-threshold CMOS design for low power digital circuits,. TENCON 2008 - 2008 IEEE Region 10 Conference, Hyderabad, India, 2008, pp. 1-5.

[3] Anand R P and Sekhar C P. Reduce Leakage Currents in Low Power SRAM Cell Structures. 2011 IEEE Ninth International Symposium on Parallel and Distributed Processing with Applications Workshops, Busan, Korea (South), 2011, pp. 33-38.

[4] Mukhopadhyay S, Kim K, Chuang CT and Roy K. Modeling and analysis of total leakage currents in nanoscale double gate devices and circuits. ISLPED '05: Proceedings of the 2005 International Symposium on Low Power Electronics and Design, 2005., San Diego, CA, USA, 2005, pp. 8-13.

[5] Thondapu C, Elakkumanan P, Sridhar R. RG-SRAM: a low gate leakage memory design, IEEE Computer Society Annual Symposium on VLSI, Tampa, FL, USA, 2005, pp. 295-296.

[6] Lu Qiang, et al. Leakage current comparison between ultra-thin Ta2O5 films and conventional gate dielectrics. IEEE Electron Device Letters,19(9): 341-342, Sep. 1998.

[7] Banu S and Gupta S. The Sub-Threshold Leakage Reduction Techniques in CMOS Circuits, 2020 International Conference on Smart Technologies in Computing, Electrical and Electronics (ICSTCEE), Bengaluru, India, 2020, pp. 223-228.

[8] Lin T, et al. Suppression of the Carbon Vacancy Traps and the Corresponding Leakage Current Reduction in 4H-SiC Diodes by Low-Temperature Implant Activation in Combination With Oxidation. IEEE Electron Device Letters, 44(4): 578-581, April 2023.

[9] Deng L, Li K and Shan W. IVATS: A Leakage Reduction Technique Based on Input Vector Analysis and Transistor Stacking in CMOS Circuits, 2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA, 2023, pp. 1-5.

[10] Deb P, Debnath B and Aryalekshmi B. N. Novel Technique to Minimize Edge Delay and Leakage Power in CMOS Adder Circuits Using 22nm Technology. 2025 3rd International Conference on Smart Systems for applications in Electrical Sciences (ICSSES), Tumakuru, India, 2025, pp. 1-4.