Research Progress on Delay Analysis and Operation Optimization Based on NAND Gates

Hanwen Zhang*

Electronic and Computer Engineering, University of York, York, YO10 5DD, United Kingdom

*Corresponding author: sdx504@york.ac.uk

Abstract. This paper systematically investigates the delay characteristics and computational performance of NAND gates across different platforms, focusing on their performance in key metrics such as delay, power consumption, area, and integration density. The benefits and limitations of various NAND structures which consisting of speed, energy efficiency, and applicable scenarios are revealed by compare with different implementation paths, including traditional CMOS, FinFET, photonic crystals, Semiconductor Optical Amplifiers (SOA), and Organic Thin-Film Transistors (OTFT). By considering the shortcomings such as drive and integration limitations in silicon-based processes, high power consumption and functional rigidity in optical logic, and performance deficiencies in flexible electronics in NAND gate development—this paper proposes four optimization paths: a hybrid NAND architecture using heterogeneous integration and negative capacitance FinFETs, an optoelectronic neuromorphic scheme combining plasmonic and memristors, a dynamic body bias 3T NAND structure for low-voltage applications, and a quasi-CMOS logic utilizing oxide-organic TFT hybrids. This research can provide theoretical references and technical directions for the design and application of high-efficiency, high-integration, and flexible electronic systems NAND gates.

Keywords: NAND gates; Delay; Power consumption.

1. Introduction

With the rapid development of the Internet of Things (IoT), edge computing, and low-power embedded systems, the requirements for digital logic gates in terms of power consumption, delay, area, and integration density have become increasingly stringent. Common CMOS technology is troubled by some limitations such as short-channel effects and increase of leakage currents at the nanoscale, which provides a direction for exploring new device structures, material systems, and even cross-technology platforms (e. g. optical computing, flexible electronics). As a widely used common logic gate, the performance optimization of the NAND gate has become an important research direction for improving overall system energy efficiency and computational speed.

In recent years, researchers have improved the performance of NAND gates from multiple levels, including device, circuit, and architecture. The main research achievements can be categorized into traditional silicon-based CMOS and its enhancement technologies, emerging devices and heterogeneous integration schemes, optical computing platforms, and flexible electronics based on organic TFT technology.

The research of traditional silicon-based CMOS technologies is focusing on improving performance of device structure and optimization of the process. Channi et al. has chosen a 3-transistor (3T) NAND gate to design a decoder circuit, which can achieve lower power consumption, and a better Power-Delay Product (PDP) compared to the usual 4T structure under a 250nm process [1]. Sinha et al. have designed compact single-device NAND and NOR structures by using Non-Aligned Double Gate FETs (NADGFET), which can achieve a 69.45% delay improvement at the 270nm scale [2]. Vishnu Vardhan et al. designed NAND gate-based adder and subtractor circuits after analysing CMOS and FinFET technologies, which reduced both power consumption and delay significantly [3]. Kuwal et al. compared the logic, power, and delay of NAND and NOR gates by using the Cadence Virtuoso tool under a 45nm process, highlighting the advantages of NAND gates in terms of speed and power consumption [4]. Della Sala et al. proposed a comprehensive ultra-low voltage NAND-based comparator that maintains good performance even at a 0.3V supply voltage [5].

The research of optical computing on NAND gates provides a different way for ultra-high-speed, low-power information processing. Based on photonic crystal ring resonators and the Kerr nonlinear effect, Khalissa et al. designed all-optical AND/NAND gates, achieving a high bit rate of 0.52 Tb/s [6]. Bagheri et al. used 2D photonic crystals to design a NAND gate which has a compact structure with high contrast ratio based on a ring resonator [7]. Kolavi and Bosu et al. both implemented optical NAND gates using Semiconductor Optical Amplifiers (SOA) and Reflective SOAs (RSOA) respectively, making them suitable for photonic FPGAs and highly parallel optical computing systems [8] [9].

Furthermore, for the emerging flexible electronics applications, Mehrolia et al. explored the implementation of NAND gates based on Organic TFTs (OTFT), which supply new possibilities for flexible electronics and low-cost sensing applications [10].

This paper investigates the feature about the timing and performance of the computation of NAND gates across different technology platforms, focusing on the analysis and evaluation of key metrics such as delay, power consumption, area, and integration density. The paper first describes and analyzes NAND gates using different design methods with various implementations including CMOS, FinFET, photonic crystals, SOA, and OTFT. After that, the advantages and disadvantages of each technology are evaluated in terms of speed, power consumption, and applicable scenarios. Finally, by considering the limitations faced by various NAND gates in performance and integration, it proposes future-oriented optimization paths.

2. Model Analysis of NAND Gate Circuits

This section will analyze and compare three typical implementation methods which contain silicon-based logic gates, Optical Logic Gates, and flexible electronic logic gates based on the systematic review of NAND gate performance optimization paths. To clearly present the structural composition and performance characteristics of each model, Fig.1 systematically compares the structure and core advantages of typical NAND gates under these three technological paths.

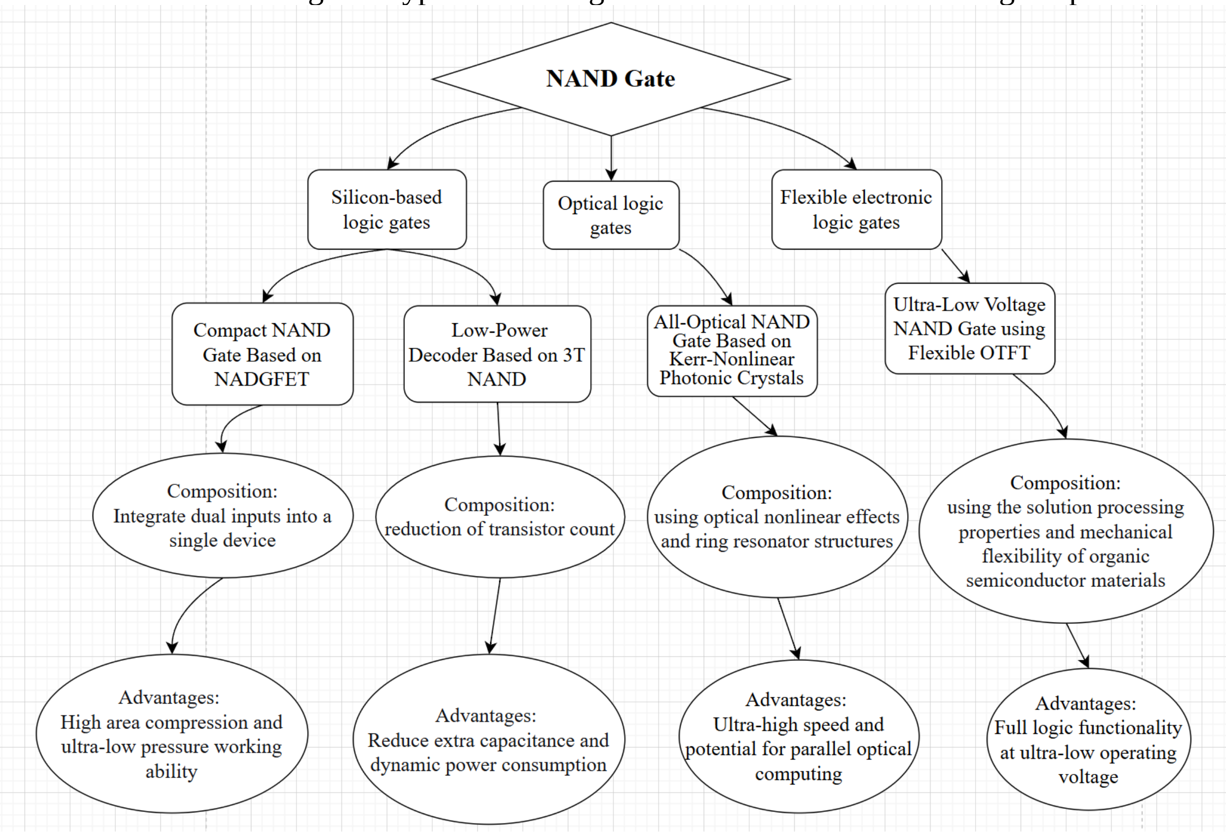

Fig.1 Summary of multi-technology path implementation models for NAND gates

2.1. Research on Performance Optimization of Silicon-Based CMOS NAND Gates

Based on the common silicon-based CMOS technology, performance optimization of NAND gates primarily extends to two dimensions which are innovative device structures and optimized circuit architectures. The former focuses on breaking the physical limitations of traditional CMOS through novel transistor structures, while the latter emphasizes performance improvements through circuit-level restructuring based on existing processes.

2.1.1 Compact NAND gate based on NADGFET

Sinha et al. used a Non-Aligned Double Gate FET (NADGFET) to develop an innovative NAND gate, which combined the logic function into a single device instead of the usual four transistors (2 PMOS and 2 NMOS). This design used input signals to different gates of the same device and improved the device structure and doping profile, implementing the NAND logic function on a single physical device. This structure significantly improves area efficiency, making it more compatible for high-density integrated circuits. Additionally, this NAND gate can operate stably at an ultra-low supply voltage of around 0.78V by optimizing materials and structure, which can reduce dynamic power consumption. Under these low-voltage conditions, it can even achieve fast, picosecond-scale propagation delays, which perform a good improvement of about 69.45% compared to similar designs and demonstrating excellent low-voltage, high-speed characteristics.

However, this NADGFET NAND gate still has several challenges in practical application. Firstly, because of its complex non-aligned double-gate structure, this structure needs a precisely nanoscale manufacture. Any small process variations can make the logic correctness drop down and may allow noise more effective by the reason that the threshold voltage does not match. Also, its poor compatibility with standard CMOS processes can make the costs of manufacturing higher and production yield lower. After that, it may be weaker than the parallel PMOS network in common gates due to only one channel branch providing the drive current. This can make signals weaker and produce some delay that is out of expected because of the limits of its ability to drive large capacitive loads or multiple following gates in real-world applications. Finally, by integrating multiple inputs into one device, the electric field strength and current density can be increased at critical points, which could affect the stability, reliability and life of the device due to some part of the device heating up.

2.1.2 Low-power decoder based on 3T NAND gate

Based on the framework optimization, the research by Channi et al. focused on improvement at the architecture of the circuit. This study used a non-standard 3-transistor (3T) NAND gate (1 NMOS + 2 PMOS) as the basic unit to construct a 2-4 decoder, comparing it with a decoder using common 4T NAND gates [1]. The 3T NAND gate, having fewer transistors, also results in less capacitance and fewer switching activity nodes. Simulation results showed that across the entire operating voltage range (2.0V-2.5V), the average power consumption of the decoder based on the 3T NAND was 0.217mW lower than the common 4T design. The Power-Delay Product (PDP) was also better for this 3T design due to its lower power consumption at nearly the same delay, showing higher energy efficiency.

Despite this, the structural optimization of the 3T NAND gate also brings some problems with performance. First, its pull-up network consists only of PMOS resistors. When the inputs are "01" or "10", the output high level attends to loss threshold voltage, leading to signal amplitude decrement. This decrement not only reduces the circuit's noise margin but may also accumulate and cause logic errors in multi-stage cascades.

Afterwards, under specific input states, both the PMOS and NMOS can be turned on at the same time, which creates a direct current path from the power supply to ground, producing additional static power consumption. Also, as the rising and falling edges are controlled by transistors of different types, the output waveform displays asymmetry, offering challenges for timing analysis and circuit convergence. These problems will totally limit the applicability of the 3T NAND gate in large-scale digital systems.

2.2. Research on NAND Gate Optimization in Optics and Flexible Electronics

In emerging areas like high-speed computing and flexible electronics, the implementation methods of NAND gates have also exceeded the common silicon-based CMOS area, showing various aspects of technological paths. In the direction of optical computing, researchers are exploring structures like photonic crystals to achieve ultra-high-speed all-optical logic operations. In the field of flexible electronics, Organic Thin-Film Transistors (OTFT) show the possibility of implementing bendable, low-cost NAND gates.

2.2.1 All-optical NAND gate based on Kerr-nonlinear photonic crystals

Khalissa et al. created a new design for an optical NAND/AND gate using a component called a two-dimensional Photonic Crystal Ring Resonator (PhCRR) [6]. Their design can change its properties with light intensity which is called the Kerr effect using silicon carbide as a special material. This allows it to work as a very fast optical switch. Because light signals respond in femtoseconds, this gate can operate at ultra-high bit rates with picosecond delays, making it much faster than common electronic devices. The design of the resonator was also improved to create a clearer distinction between the on and off' logic states, making it more reliable. Moreover, its small size makes it easy to build into larger optical chips with other components like waveguides.

Even though the structure has many advantages, this high speed also produces some difficulty. The gate needs a strong and concentrated optical power density to switch the structure, the required power levels are much higher than other usual electronic logic gates. It would be difficult to build a complex chip with thousands of these gates because of the large requirement of the power, which also limits its use to specialized, small-scale and high-speed applications. Additionally, the function of the gate is fixed, so it cannot be reprogrammed, this will also be a problem for flexible computing systems. In high density combination chips, the accuracy would be affected when the powerful light signals generate heat by blocking with each other. Furthermore, the efficiency would be lower when converting light to electricity and produce delay, because optical systems still need to link with electronic parts, and the speed benefit can be lost.

2.2.2 Ultra-low voltage NAND gate using flexible OTFT

Mehrolia et al. developed a flexible transistor (TFT) using an organic polymer called P3HT. They successfully built and tested this device on a flexible plastic PET model and used it to create a full digital logic system, including NAND gates [10]. This organic transistor operates at a very low voltage (-2V) and is highly flexible, making it ideal for wearable technology or electronic skin. It uses solution-based methods like spin-coating for the process of manufacturing, which the temperature is lower and much cheaper than silicon chip production. So, this structure can achieve large-area, low-cost production. The NAND gate correctly performed its logic function for all possible inputs in the simulations test, meaning that organic electronics can be used to build digital circuits.

However, these organic transistors might have some trouble when performing in practice. The organic materials have poor ability to conduct electrical charge slowly that a single inverter has a delay of 3.7 ns and make the drive current weaker. Which means they are thousand times slower than modern silicon transistors. So, the circuit might not be the best choice when working at high speed. Also, since the drive current is weak, it is difficult to power other components, meaning that the circuit might fail in a real device even if it works in the simulation test. In addition, the structure might be difficult to work stable in a long time because organic materials can be easily affected by the environment like oxygen or other factors. The manufacturing process can affect the clear consistency of the timing between transistors, it would be hard to use in large, complex circuits. These problems will limit their practical use in the real world.

3. Scheme Design and Optimization

3.1. Design Challenges and Countermeasures for NADGFET NAND Gate

To solve the process difficulty and increase the performance of NADGFET, a hybrid NAND architecture plan based on heterogeneous integration technology can be considered. This plan uses advanced packaging technology to integrate high performance nanosheet FETs with common FinFET PMOS instead of using the double-gate structure that is not aligned and difficult to produce. The plan can apply some features such that the nanosheet FET can use multi-gate to provide strong pull-down drive capability, and the parallel FinFET PMOS form an effective pull-up network. This heterogeneous integration approach is more reliable, it can largely improve the drive performance of the overall circuit and does not need complex processes, Also the symmetrical circuit structure can keep working well when facing process variations.

3.2. Optimization Scheme for 3T NAND Gate Design

To solve the problems of level decrement and static power consumption in the 3T NAND gate, an improved architecture combining negative capacitance FinFETs and dynamic body bias technology can be introduced. This plan uses the steep switching feature of negative capacitance FinFETs to improve output level integrity; also, through a simple control circuit, when operating the conditions where input combinations can be loss, a negative body bias is dynamically applied to the NMOS to greatly increase its threshold voltage, thereby completely turning off the direct current path and removing static power consumption. This method only needs to add a small amount of control circuitry to improve its disadvantages and keep the low-cost advantage of the 3T structure, making it better for low-voltage, high-efficiency circuit design.

3.3. Scheme Optimization for Photonic Crystal NAND Gate

To develop the high-power consumption and functionality of the photonic crystal NAND gate, a new neuromorphic computing way using plasmonic improvement and optoelectronic fusion can be considered. This plan uses optical pulses to implement computing functions like the brain instead of using the common optical logic method. the plasmonic effect reduce the optical field to the nanoscale, which can also decrease the power required for nonlinear operations; the improved photonic structure can serve as a programmable synaptic unit, working with memristors and perform multiply-accumulate operations efficiently on optical pulses in a crossbar array. This hybrid optoelectronic architecture achieves high-efficiency computing and break through the limitations of fixed logic function, which might be helpful for building adaptive optical computing systems.

3.4. Scheme Optimization for Organic TFT NAND Gate

To solve the problems of slow speed and weak drive ability in organic TFT NAND gates, a quasi-CMOS architecture with hybrid integration of oxide TFTs and organic TFTs can be referred to. This plan keeps the easily processable P-type organic TFT in the pull-up path and introduce high-mobility N-type metal-oxide TFTs (e.g., IGZO) in the pull-down path, using low-temperature processes to achieve complementary integration on flexible substrates. This design is expected to combine the speed advantage of oxide semiconductors with the flexible characteristics of organic materials, greatly improving circuit response speed and drive ability, and developing static power consumption and output level integrity, providing a more practical technological path for medium-performance flexible electronic applications.

Based on the analysis of key problems and optimization directions faced by various models, Table 1 further summarizes the shortcomings of each NAND model and the corresponding improvement suggestions, providing a reference for following system design and technology selection.

Table 1. Comparison of NAND gate optimization models and improvement schemes

Model Category	Main Shortcomings	Optimization Suggestions
NADGFET NAND	High process difficulty, weak drive capability, low reliability	Adopt heterogeneous integration plan, combining nanosheet FET and FinFET PMOS to increase drive ability and process compatibility
3T NAND	Output level decrement, presence of static power consumption	Introduce negative capacitance FinFET and dynamic body bias technology to eliminate direct current path and improve level integrity
Photonic Crystal	High power consumption, fixed function, lack of flexibility	using neuromorphic computing architecture, combining plasmonics and memristors to achieve low-power programmable optical computing
Organic TFT NAND	Slow speed, weak drive capability, poor stability	Construct oxide-organic TFT hybrid complementary structure to improve mobility and power consumption & level issues

4. Summary

This paper has systematically studied the timing characteristics and computational performance of NAND gates across multiple technology platforms, focusing on their performance in main metrics such as delay, power consumption, area, and integration density. Through a review and comparison of implementation paths including common silicon-based CMOS, FinFET, photonic crystals, SOA, and OTFT, it has showen the core challenges faced by various NAND gates in the pursuit of high performance, low power consumption, and high integration. The silicon-based path is limited by physical scaling limits and process complexity, and the optical path faces the difficulty of high-power consumption and functional flexibility. Also, the flexible electronics path is limited by the performance of materials. In response to the above challenges, this paper proposes forward-looking optimization ideas.

To improve the performance of NAND gates, different technological paths are developing towards their outstanding abilities. The silicon-based route can extend Moore's Law through heterogeneous integration and new devices and focusing on energy efficiency improvement; the optical route abandons common logic, turning to neuromorphic optical computing to open specific application scenarios; flexible electronics can choose hybrid integration to achieve better performance and maintain its advantages.

In summary, the future development of NAND gates will no longer rely on the linear optimization of a single technological route. Instead, based on the requirements of the application scenario (e.g., high-speed computing, edge inference, flexible sensing), cross-technology collaborative optimization of silicon-based, optical, and flexible platforms is required. This multi-dimensional design method may reveal the direction of the next generation of high-efficiency, high-integration, and flexible digital information systems.

Reference

[1] Channi M K, Kumar M. Design and Evaluation of Low Power 2 to 4 Decoder Circuit Using Three and Four Transistors NAND Gates. 2024 International Conference on Integrated Circuits, Communication, and Computing Systems (ICIC3S), IEEE, Una, India, 2024.

[2] Sinha A K, Sangam S L, Melek L A P. Universal Gate Design Using Non-Aligned Gate Transistors: A Performance Evaluation in TCAD. 2024 IEEE Silchar Subsection Conference (SILCON 2024) , IEEE, Agartala, India, 2024.

[3] Vardhan B V, Khadir M D, Sunnyhith K. Design and Implementation of Low Power NAND Gate Based Combinational Circuits Using FINFET Technique. 2023 14th International Conference on Computing Communication and Networking Technologies (ICCCNT), IEEE, Delhi, India, 2023.

[4] Kuwal V, Yadav S S, Dandapat A. Analysis of the Universal Gates based on the Comparative Factors of Delay Propagation, Average Power Dissipation and Logical Effort. 2021 2nd International Conference for Emerging Technology (INCET), IEEE, Belagavi, India, 2021.

[5] Sala.R D, Bocciarelli C, Centurelli F, Spinogatti V, Trifiletti A. A Novel Ultra-Low Voltage Fully Synthesizable Comparator exploiting NAND Gates. 2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), IEEE, Valencia, Spain, 2023.

[6] Khalissa C, Redha L M, Fateh L. Design of all optical AND/NAND logic gates with high Performance using the nonlinear Kerr effect. 2024 8th International Conference on Image and Signal Processing and their Applications (ISPA), IEEE, Biskra, Algeria, 2024.

[7] Bagheri M, Karimi G. Design and Simulation of a NAND Gate based on 2D Photonic Crystals. 2024 Third International Conference on Distributed Computing and High Performance Computing (DCHPC), IEEE, Tehran, Iran, Islamic Republic of, 2024.

[8] Kolavi S, Roy U M. Design and Simulation of SOA based Optical NAND gate for photonics FPGA. 2021 2nd International Conference for Emerging Technology (INCET), IEEE, Belagavi, India, 2021.

[9] Bosu S, Bhattacherjee B. Dibit-based NAND gate using Reflective Semiconductor Optical Amplifier. 2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON), IEEE, Kolkata, India, 2022.

[10] Mehrolia M S, Mishra A K, Singh R. Implementation of Digital Logic Gate Families using Low Operating Flexible Organic TFT based on Innovative Compact Modeling Approach. 2025 3rd IEEE International Conference on Industrial Electronics: Developments & Applications (ICIDeA), IEEE, Bhubaneswar, India, 2025.