Research into Optimizing the Performance of NAND Logic Gates in Terms of Delay and Power Consumption

Kaiming Chen[1, 2, *]

[1] Houston International Institute, Dalian Maritime University, Dalian, 116085, China

[2] Houston International Institute, University of Houston, Houston, 77204, America

*Corresponding author: kchen50@CougarNet.UH.EDU

Abstract. NAND logic gates constructed with CMOS/MOSFET technology in digital integrated circuits are susceptible to degradation. Optimizing latency and power is vital to enhance performance. In order to optimize latency and power consumption in NAND logic gates, this paper conducts a systematic analysis of recent research on these parameter optimizations. There are three main ways to reduce latency. The first is to use all-optical structures with MIM waveguides. The second is to increase the frequency of RF MEMS resonators. The third is to control devices at the RFET level. The following three core strategies for power optimization are examined in this study. The initial technologies under consideration are those which combine floating-gate metal-oxide-semiconductor field-effect transistor (FGMOS) and carbon nanotube field-effect transistor (CNTFET). The second is all-optical architectures integrated with passive diffractive networks. CMOS complementary structures represent the third strategy. The study identifies the limitations of these approaches. These include constraints in traditional and emerging process technologies, and limitations in delay-power optimization. In order to address these shortcomings, a number of targeted strategies have been proposed, including the improvement of environmental adaptability, the optimization of circuit structures and the innovation of design techniques. The present research provides systematic guidance and theoretical support for advancing technologies related to the delay and power optimization of NAND logic gates.

Keywords: NAND logic gate; CMOS/MOSFET technology; delay-power optimization.

1. Introduction

The performance of devices manufactured using CMOS/MOSFET technology with dimensions below 20nm (for example, NAND logic gates) is being impacted by the ongoing reduction in the size of technology nodes in the domain of digital integrated circuits [1]. In order to improve their performance, they need to be optimized. There are two main ways to improve the performance of NAND logic gates, and both of these methods are outlined below. The first way to do this is to reduce the propagation delay. The second way is to reduce power consumption, which can be achieved in a number of ways. A close relationship between delay and power consumption has been identified. To improve circuit performance, it is crucial to optimize NAND gate delay and power consumption in high-frequency applications and scenarios with low power consumption. This also offers advantages such as extending device battery life and reducing thermal noise.

Next-generation computing frameworks must have two fundamental prerequisites: delay and power consumption. Significant progress and innovations have been achieved. These have been in optimizing the delay and power consumption of NAND logic gates. Power consumption was successfully reduced by Sevgi and Serdar through the replacement of standard resistors in NAND gates with current- and voltage-controlled memristor simulators to construct circuits [2]. NAND gate power consumption was reduced by Uma and Mansi through the synergistic employment of two distinct non-traditional semiconductor technologies [3][3]. The proposal by Kang et al. of a dual-cell height complementary field-effect transistor-based NAND gate design resulted in effective reduction of NAND gate power consumption [4]. By having trap-clearing pulses optimized, channel-injection interface trap charges were selectively removed by Kim et al., which resulted in post-read/write delays being resolved and NAND device power consumption being reduced [5]. The studies show that there are different ways to make NAND better at storing information quickly and using less power. This underscores the significant value of conducting a systematic review in this field.

This paper discusses how scientific research can enhance NAND logic gates' performance, speed and energy consumption. It outlines technologies developed for delay and power optimization, and discusses the big problems in this area. It also compares ways to make things better in terms of time and energy. Finally, the paper proposes solutions to reduce NAND gate delay and energy consumption. Overall, this research provides systematic reference. It also provides theoretical support. This is for the future development of NAND logic gate delay and power optimization technologies.

2. Method

This section analyses methods for reducing the delay and power consumption of NAND gates. It examines current optimization approaches. Regarding delay reduction, three strategies are introduced: all-optical structure optimization based on MIM waveguides, frequency enhancement mechanisms leveraging RF MEMS resonators, and device-level characteristic control using reconfigurable field-effect transistors (RFETs). Regarding power consumption reduction, three approaches are discussed. The first is synergistic application of non-traditional semiconductor technologies (FGMOS and CNTFET). The second is all-optical architecture design based on passive diffraction networks. The third is complementary CMOS structure optimization integrating NMOS and PMOS.

2.1. NAND Gate Delay

2.1.1 All-optical NAND gates using MIM waveguides

Charles et al. proposed an all-optical NAND gate based on a 2D MIM waveguide, compact size optimization, and a simplified Y-shaped NAND gate structure to reduce its delay [6]. MIM (Metal-Insulator-Metal) waveguides are structures composed of two metal electrodes with an insulating layer between them. MIM waveguides have a simple structure. They can confine light at the nanoscale. This achieves sufficient transmission distances and low crosstalk characteristics. This makes them ideal for various ultra-compact devices. In this research, the highly efficient light confinement and guidance capability reduces signal propagation delay within the NAND gate. The all-optical NAND gate performs logical NOT operations using optical signals. In this study, the NAND gate also simplifies the Y-shaped power combiner structure. This approach endows the NAND gate with an efficient circuit structure. It also gives it high-speed optical computing capability. This achieves reduced NAND gate delay.

2.1.2 Resonant frequency enhancement mechanism

Mahdi and Reza proposed a novel logic gate architecture that integrates RF MEMS resonators to implement NAND gates, which is a significant development in the field [7]. The architecture is designed to reduce NAND gate delay by increasing the resonant frequency of the resonators within the resonator network, which act as processing elements. The mechanism behind this frequency enhancement is based on the positive correlation between delay time and resonant period. At the same number of cycles, a higher resonant frequency means a smaller proportion of time per cycle. This results in lower overall delay. The effect of frequency enhancement on delay improvement was the focus of the simulation experiments in this study. The results show that there is a relationship between the resonant frequency and delay. This means that using higher-frequency resonators can reduce the delay of this NAND gate architecture even more. The research establishes a scheme for reducing delays in RF MEMS resonator-based NAND gates. This is achieved through a three-tiered technical approach that the three processes are frequency enhancement, cycle optimization and signal amplification.

2.1.3 Reconfigurable field-effect transistors

Giulio et al. proposed using reconfigurable field-effect transistors (RFETs). They suggested using them as a technological platform [8]. The aim was to achieve delay optimization for NAND gates.

RFET integrates n-type and p-type functions into a single device, maintaining symmetry. The design realizes this without changing the geometric size of the device, eliminating the obstacles of device-level delay optimization. The triple-gate structure supports switching operating modes through gate signals. This method can optimize the current path without changing the structure. Design flexibility has improved. The three-door structure consists of a control door, a polarization door and a control door. A three-stage design method is used to construct a NAND cell that can be modified at low voltage. The method includes connecting series branches and applying the same signal to the control gate to slow down the PUN charging. This configuration is designed to ensure low latency even under complex circuit conditions. Valuable information for the design of high-performance logic circuits is provided by this study.

2.2. NAND Gate Power Consumption

2.2.1 Collaborative adoption of non-traditional semiconductor technologies

Uma and Mansi's NAND gate design used two non-traditional semiconductor technologies: floating-gate metal-oxide-semiconductor field-effect transistors (FGMOS) and carbon nanotube field-effect transistors (CNTFET) [3]. This research combines the adjustable threshold voltage of FGMOS with the carrier ballistic transport and high scalability advantages of CNTFET to create FG-CNTFET technology. NAND gates designed using FG-CNTFET technology achieve better power optimization than those designed using non-traditional semiconductor technology alone. FGMOS reduces the number of transistors and voltage requirements in NAND gates, while CNTFET lowers leakage current and latency. The integration of these two technologies achieves dual optimization. This is because it significantly reduces overall NAND gate power consumption and energy delay. As a result, both ultra-low power consumption and ultra-short latency are realized.

2.2.2 All-optical NAND Gates based on diffraction networks

Yi et al. proposed designing a fully optical NAND gate that can be cascaded using a diffractive neural network, encoding the logical values of the diffractive NAND gate's input and output planes through the relative optical power of two spatially separated aperture [9]. The core mechanism for optimizing power consumption in this study is the use of a passive diffractive network. This network is used to eliminate the dynamic power consumption of the NAND gate. Only illumination light is required during operation. This means that no additional energy is required. Conventional optical logic gates, on the other hand, rely on active devices or nonlinear effects, meaning they need a continuous power supply to maintain states and consume a lot of power. The architecture was built on to optimize the design of a diffractive neural network composed of four passive layers. It performed XOR operations using light diffraction. This was achieved in an all-optical manner. A set of cascade arrays is also constituted by these diffractive NAND gates. They are used to perform complex logical operations for data processing and decision-making. Moreover, an all-optical half-adder has been developed, which represents a significant landmark in this domain.

2.2.3 CMOS technology combining different metal oxide semiconductors

A NAND gate based on complementary metal-oxide-semiconductor (CMOS) technology was proposed by Angelo et al [10]. This configuration uses N-type (NMOS) and P-type (PMOS) transistors, which means it can use low voltage and not much power. The study examines power optimization mechanisms from static and dynamic perspectives. A static state is achieved if the configuration of the complementary NMOS and PMOS transistor pairs is symmetrical. Only one transistor conducts, stopping the others from doing so. This process stops current paths and reduces static power consumption. Research shows that stability at lower voltages is maintained by CMOS structures during dynamic operation. Better efficiency in storing and releasing energy during logic switching reduces energy consumption. This design aims to optimize power efficiency and performance and preserve logical stability. This is good for low-power NAND gates too.

Table 1 lists the core technical approaches for optimizing NAND logic gates' latency and power consumption. It also summarizes each method's technologies, including mechanisms for reducing latency and power consumption.

Table 1. Comparison of NAND Logic Gate Delay and Power Consumption Optimization Schemes

Classification	Name	Core Technology	Features
NAND Gate Delay	All-Optical NAND Gates Using MIM Waveguides	2D MIM Waveguide, Combiner	Leveraging the efficient light confinement and guidance capabilities of MIM waveguides.
	RF MEMS Resonator NAND Gate	RF MEMS Resonator	Increase the resonant frequency to reduce latency through“frequency enhancement, cycle optimization, and signal amplification.”
	RFET NAND Gate	Triple-Gate RFET	Eliminate latency barriers at the device level; optimize current paths through mode control, maintaining low latency with a three-step design approach.
NAND Gate Power Consumption	FG-CNTFET Cooperative Technology NAND Gate	FGMOS and CNTFET	FGMOS reduces transistor count and voltage requirements; CNTFET minimizes leakage current.
	Diffraction Network All-Optical NAND Gate	Passive Diffractive Neural Network	Passive diffractive networks eliminate dynamic power consumption; optimized structures enable logic cascading and complex operations.
	CMOS Complementary Structure NAND Gate	NMOS and PMOS Symmetrical Complementary Structure	Static: Only one transistor is conducting, with no continuous current path; Dynamic: Low-voltage operation reduces energy consumption during charge and discharge cycles.

3. Discussion

3.1. Challenges

3.1.1 Process challenges in traditional and emerging technologies

Regarding the three representative models discussed in NAND Gate Power Consumption: FG-CNTFET cooperative technology NAND gates, CMOS complementary structure NAND gates, and diffraction network all-optical NAND gates. While these models theoretically achieve the core goal of power optimization, emerging technologies for enhancing NAND gate performance commonly face process challenges, along with difficulties in controllability and parameter stability. FG-CNTFET cooperative technology NAND gates suffer from random growth orientation and inconsistent chirality factors during carbon nanotube fabrication. Furthermore, process variations easily disrupt the capacitive matching between the floating gate and carbon nanotube channel, undermining their ultra-low power design objectives. Diffractive network all-optical NAND gates suffer from errors in nanoscale patterning precision, aperture size, and spacing during microfabrication of the diffractive layer. These errors cause phase distortion and power loss during optical signal propagation. During practical testing of CMOS-NAND gates, variations in PMOS and NMOS gate oxide thickness are susceptible to process fluctuations. The same is true of source/drain doping concentration. The change in the speed at which transistors switch between conduction and cutoff states increases the static power consumption that was originally optimized.

3.1.2 Balancing delay and power consumption in NAND gates

The three representative models were discussed in NAND Gate Delay. MIM waveguide all-optical NAND gates, RF MEMS resonator NAND gates and RFET NAND gates. These models theoretically achieve the core objective of delay optimization. However, they face inherent difficulties. These difficulties are in reconciling the fundamental trade-off between delay and power consumption. This is when they are optimizing NAND gate performance. The MIM waveguide all-optical NAND gate requires low delay. However, the passive diffraction layer design adopted to reduce optical signal transmission power consumption increases optical power loss. If compensation is forced by enhancing incident light power, the overall device energy consumption is further elevated, with the delay-power balance being disrupted. To achieve low latency, RF MEMS resonator NAND gates require an increased resonant frequency. However, higher resonant frequency increases mechanical vibration energy consumption. Making the drive voltage lower to control power use can make the resonant frequency unstable, which can make the delay higher. RFET NAND gates utilize triple-gate control for low latency. However, the adoption of a high VT mode for the reduction of static power consumption results in an increase in device latency. Switching to a low VT mode to improve latency, in turn, leads to increased power consumption.

3.2. Solution

3.2.1 Enhance environmental adaptability

For the three low-power optimization models mentioned in Section 3.1.1—the FG-CNTFET cooperative technology NAND gate, the diffraction network all-optical NAND gate, and the CMOS complementary structure NAND gate—issues such as weak environmental adaptability and lack of performance optimization (e.g., delay, power consumption, stability) can be addressed through solutions like environmentally robust design and multivariable optimization algorithms.

1) For the environmental adaptability of FG-CNTFET-based NAND gates, voltage-robust circuits can be optimized by incorporating voltage clamping modules at the input stage. These modules leverage the capacitive voltage-dividing characteristics of multi-input FGMOS. When VDD fluctuations occur during operation due to process variations, the clamping modules stabilize the floating gate voltage, preventing power surges.

2) The environmental adaptability of the diffractive network all-optical NAND gate can be optimized. This can be done by adopting an anti-noise optical design. This design solves the issue by adding a narrowband filter and a spatial light modulator (SLM) to the input plane. This enables two functions: filtering out unwanted light and modifying the intensity of the light field. This makes the environment adaptable and reduces error rates resulting from process variations.

3) The design of CMOS complementary NAND gates incorporates a redundant transistor matrix to improve environmental adaptability. A fuse-based repair technique is used to dynamically adjust the number of transistors. Slow switching speed may be due to process deviation. Connecting the various parts of the redundant PMOS gate with a fuse improves effective conduction width. This has been proven to compensate for performance imbalances, thereby improving circuit stability and energy efficiency.

3.2.2 Optimized circuit structure and innovative design techniques.

The delay and power consumption of NAND logic gates are not solely determined by device performance. Circuit structure is equally critical. By optimizing circuit structures and employing innovative design techniques, a balanced trade-off between delay and power consumption in NAND gates can be achieved.

1) MIM waveguide all-optical NAND gates can achieve this balance by optimizing waveguide structures and co-designing with diffraction layers. The insulator layer material in the MIM waveguide is replaced with a higher refractive index material. This is used in place of the conventional material. It is used in this way while maintaining the original simplified structure. A gain medium is added to the passive diffraction layer. This forms a composite structure. The gain medium compensates for optical signal transmission losses, reducing optical power requirements while ensuring response time.

2) Designs can be created for making RF MEMS resonator NAND gates better. These designs will make the frequency more stable and control how much power is used. The single resonator network is reconfigured into a master-slave dual-resonator array structure. The master resonator employs high-stiffness materials. This maintains a high resonant frequency for low latency. The slave resonator uses low-power piezoelectric materials. These provide stable vibrational energy supplementation to the main network. The high-frequency characteristics of the master resonator are preserved by this design while mechanical vibration energy consumption is reduced, achieving a balance between low latency and low power.

3) To control the gates and optimize the path of RFET NAND gates, a coordinated approach combining gate signal regulation and dynamic input signal processing can be adopted. Series-connected RFET branches can be consolidated into dual-control-gate RFETs. Mode switching is synchronized via unipolar gate signals in these. This reduces transistor count. The application of dynamic signals to the steering gate allows low VT mode to be used in low-latency scenarios and high VT mode in low-power ones. This trade-off is established between latency and power.

These optimizations focus on simplifying structures and integrating innovations to minimize NAND gate power consumption and latency. Table 2 provides an overview of the constraints and enhancement methods of the various optimization models. The table gives a concise overview of the study's key findings and categorizes the subjects' main issues and areas for improvement across four dimensions.

Table 2. Shortcomings of NAND Logic Gate Optimization Models and Corresponding Solutions

Optimization Direction	Model Name	Core deficiency	Targeted Innovation Recommendations
Reduce power consumption	All-Optical NAND Gates Using MIM Waveguides	Random carbon nanotube growth; process variation sensitivity.	Optimize voltage-robust circuit via multi-input FGMOS capacitive voltage division
Reduce power consumption	RF MEMS Resonator NAND Gate	Microfabrication errors in diffraction layer (nanopatterns, aperture size/spacing).	Add narrowband filters and SLMs to filter stray light and correct input light intensity.
Reduce power consumption	RFET NAND Gate	PMOS and NMOS gate oxide thicknesses sensitive to process variation.	Use redundant transistor arrays; adjust count via fuse-based repair
Reduce delay	FG-CNTFET Cooperative Technology NAND Gate	Passive diffraction layer: increased incident light disrupts delay-power balance.	Replace MIM waveguide insulator with higher-refractive-index material; add gain medium.
Reduce delay	Diffraction Network All-Optical NAND Gate	Adjusting resonant frequency/drive voltage disrupts delay-energy balance.	Master resonator (high-stiffness material for low delay); slave resonator (low-power piezoelectric for stable energy).
Reduce delay	CMOS Complementary Structure NAND Gate	High VT: higher delay; Low VT: lower delay but higher power.	Convert series branch to dual-control-gate RFET; apply dynamic signals to steering gate

4. Summary

This study analyses NAND logic gate developments to improve latency and power consumption. Three delay improvement methods are summarized below. The first uses an all-optical structure based on MIM waves. The second uses RF MEMS resonators and a frequency optimization mechanism. The third uses RFET devices. Three strategies are in place. They are designed to improve power. The first integrates FGMOS and CNTFET. The second designs an all-optical structure based on a negative refractive diffraction grating. The third improves the CMOS structure. Each method's technical principles and performance characteristics are elucidated using multiple comparisons. The research identifies two challenges to be solved in NAND gate optimization. First, application limitations must be considered. These include the lack of controllability of carbon nanotubes in FG-CNTFET technology. Then there are fabrication precision deviations in all-optical structures. And finally, there is poor parameter stability in CMOS devices. Second, there is the difficulty of balancing latency and power consumption. This includes the conflict between low latency and optical power loss in MIM waveguide structures. There is also the trade-off between frequency and energy consumption in RF MEMS resonators. And there are the adverse performance effects caused by triple-gate control in RFETs.

This study proposes targeted solutions to address the aforementioned shortcomings. Voltage-robust circuits, noise-resistant optical schemes and process deviation compensation mechanisms were designed to enhance device performance stability in complex environments, with these measures being taken due to insufficient process and environmental adaptability. Achieving dynamic coordination in the face of inadequate delay-power balance required optimising the circuit structure and coming up with new technologies. This included the composite design of MIM waveguides and gain media, energy management in RF MEMS master-slave dual-resonator arrays, and synergistic control of RFET dual control gates with dynamic steering gates. These measures effectively eliminate redundant energy consumption and latency, providing a viable pathway for NAND logic gates to simultaneously meet low-latency and low-power requirements across diverse application scenarios.

References

[1] Rahin A B, Kadivarian A, Dadgar M. GNRFET-based Voltage Controlled Ring Oscillator Using GDI NAND Gate. 12th National Conference on Electrical Engineering, Islamic Azad University of Shahr Majlesi, Isfahan, Iran, Aug. 2023.

[2] Gürsul S, Hamamcı S E. Investigation of power consumption effect of various memristor emulators on a logic gate. European Journal of Technique (EJT), 2021, 11(2): 200-208.

[3] Sharma U, Jhamb M. Variability aware ultra-low power design of NOR/NAND gate using non-conventional techniques. Engineering Research Express, 2024, 6(1): 015301.

[4] Kang W C, et al. A complementary FET (CFET)-based NAND design to reduce RC delay. IEEE Electron Device Letters, 2022, 43(5): 678-681.

[5] Kim G, et al. Optimizing De-Trap Pulses in Gate-Injection Type Ferroelectric NAND Cells to Minimize Read After Write Delay Issue. IEEE Electron Device Letters, 2024, 45(12): 2359-2362.

[6] Charles I, et al. Enhanced all-optical Y-shaped plasmonic OR, NOR and NAND gate models, analyses, and simulation for highspeed computations. Optical and Quantum Electronics, 2022, 54: 330.

[7] Attar M, Askari M R. High speed universal NAND gate based on weakly coupled RF MEMS resonators. Microsystem Technologies, 2024, 30(3): 319-329.

[8] Parandin F, Malmir M. Low delay time all optical NAND, XNOR and OR Logic gates based on 2D photonic crystal structure. Journal of Electrical and Computer Engineering Innovations (JECEI), 2020, 8(1): 1-8.

[9] Luo Y, Mengu D, Ozcan A. Cascadable all-optical NAND gates using diffractive networks. Scientific Reports, 2022, 12(1): 7121.

[10] Beltran Jr A A, Nones K, Salanguit R L, Santos J B, Santos J M R, Dizon K J. Low Power NAND Gate–based Half and Full Adder/Subtractor Using CMOS Technique. Journal of Robotics and Control (JRC), 2021, 2(4): 252-257.