Effects of Different Processes and Structures on CMOS Device Characteristics

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Abstract. CMOS technology is the basis of integrated circuit technology, and the characteristics of CMOS technology affect the function of the circuit. If the MOSFETs that compose the CMOS circuit use the voltage-current characteristic to amplify the signal in the “saturation region”, if they use the “variable resistance region” to work just like a variable resistor, or if they use the characteristic of threshold voltage as a voltage reference chip. These characteristics fundamentally depend on the manufacturing process employed. This paper reviews the research progress in silicon-based integrated circuit manufacturing process technology. The analysis covers the key characteristics of mainstream complementary bipolar technology, BiCMOS technology, and non-planar structure processes in the industry, along with their impact on CMOS device properties, including feature frequency. This paper aims to investigate the impact of different manufacturing processes on the development of CMOS devices, analyzing their specific effects on device characteristics and the underlying reasons.

Keywords: Complementary bipolar technology, BiCMOS technology, FinFET.

1. Introduction

CMOS devices are common components in circuits that play a crucial role. For example, thousands of P-MOS and N-MOS transistors form these practical logic circuits, within which functions such as logic operations or signal amplification can be implemented. At the same time, demand for CMOS devices has also increased, with higher requirements for their speed, power consumption, and size. The speed of CMOS devices generally refers to the switching speed of transistors. This characteristic determines the rate at which logic gate digital levels change, thereby determining the magnitude of digital signal transmission delay. The power consumption of CMOS devices determines the static and dynamic power consumption of the entire circuit or machine. Excessive power consumption may cause electronic components to overheat, potentially damaging the entire device or causing temperature drift in its components. This, in turn, leads to signal errors in the circuit, particularly affecting analog signals. The size of CMOS devices determines their level of integration. Only by reducing the size of transistors can more transistors be placed on a single chip, thereby increasing its integration level. To meet the demand for higher integration level, the transistor dimensions of MOSFETs are continuously shrinking. However, as the dimensions decrease, particularly when the gate length shrinks to the deep submicron range, performance degradation occurs. This phenomenon is known as the “Short-Channel Effects”. Additionally, there are effects such as the small-size effect, the mobility modulation effect, the Drain-Induced Barrier Lowering effect, and HIGH-Field effects [1,2].

Unlike digital integrated circuits, which pursue higher integration levels using advanced CMOS processes and have closely followed Moore's Law for an extended period, the development of analog integrated circuit processes does not solely depend on the reduction of device feature sizes. To meet the specialized requirements of analog integrated circuits for high voltage, high speed, high precision, and low power consumption, their manufacturing processes often incorporate multiple active devices such as bipolar and CMOS, along with high-performance passive devices necessary for achieving essential analog functionality [3]. In addition, analog products often demand output signals with stringent requirements and this accuracy is obtained by an accurate match between the circuit design

and manufacturing process. As a result, the development of analog integrated manufacturing processes has been largely processing technology change driven and a number of process types have been developed.

Complementary bipolar technology, BiCMOS technology and other non-planar device processes like FinFET structures represent more advanced and complex techniques developed by adding additional steps and modules to the complementary process, namely the CMOS process. These distinct processes exert varying effects on the characteristics of CMOS devices.

This paper aims to describe the specific principles of the complementary bipolar technology, BiCMOS technology and FinFET structure proposed above. It explains the fundamental reasons why these technologies can improve CMOS devices, details the impact of different processes on specific CMOS device characteristics, and compares the advancements these processes offer over previous technologies. This aims to clarify the objectives for improving CMOS devices and the future direction of such improvements.

2. Complementary Bipolar Technology

Bipolar technology was the earliest integrated circuit manufacturing process. Thanks to its advantages of high speed, low noise, and high current drive capability, it remains one of the key specialty processes for analog integrated circuits today. Compared to non-complementary NPN bipolar processes, incorporating complementary high-performance PNP transistors significantly enhances circuit operating range, reduces circuit complexity, and improves drive capability [4,5].

Traditional PN-junction isolated standard bipolar technology is widely used in various general-purpose operational amplifiers. In traditional manufacturing processes, it is relatively easy to produce NPN transistors that meet specifications, but it is often difficult to provide a matching PNP transistor with equivalent parameters. The circuit contains only two types of transistors—lateral transistors and vertical transistors, as shown in Figure 1. PNP transistors manufactured using this process employ either lateral PNP or substrate PNP structures. This results in relatively high base resistance for transistors of this configuration, limiting their application in high-frequency domains [4].

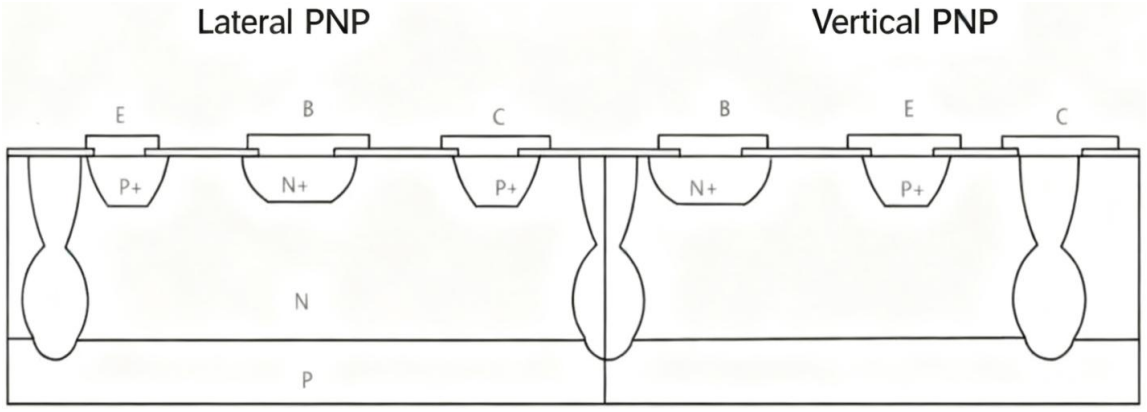


Figure 1. Schematic Diagram of Horizontal PNP and Vertical PNP Structures

From the structure, it can be seen that traditional PNP transistors typically employ either a lateral or substrate PNP configuration. Its structure features an extremely wide base width—the distance between the two P+ regions of the emitter and collector—far exceeding the diffusion control precision of the vertical N-channel. This results in a very low β (DC current gain). Under these conditions, the transistor's input current exhibits low control efficiency over the output current, significantly impacting CMOS performance. Compared to earlier technologies, complementary bipolar PNP transistors employ a fully vertical structure similar to NPN transistors, exhibiting notable characteristics such as high speed and minimal β decay under high current conditions, which improve performance. To achieve this, the complementary bipolar process incorporates other complex structures. For example, NBL (N-type buried layer) and PBL (P-type buried layer), along with a deep

diffusion isolation layer, were introduced. Among these, the vertical structures of PNP transistors can be broadly categorized into three forms: the free-collector process structure, the N-type epitaxial complementary process structure, and the P-type epitaxial complementary process structure. Taking the N-type epitaxial complementary process as an example, Figure 2 shows a schematic diagram of the multi-layer structure of an N-type epitaxial vertical PNP transistor.

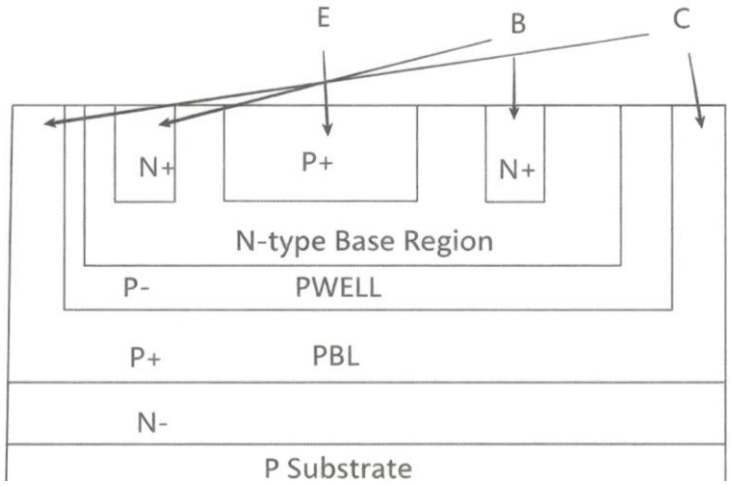


Figure 2. PNP Transistor Structure

The P-type well (PWELL) interfaces with the P-type buried layer (PBL) to form the collector region of the PNP transistor. PSINK injection around the PWELL reduces Rc and serves as the collector lead. This allows the P-type buried layer to provide a relatively low-resistance path for the PNP collector current. This enhances the performance of the PNP transistor to match that of the NPN transistor, reducing its base resistance and increasing its characteristic frequency. The effect of this process on the characteristic frequency of CMOS devices enables them to function in higher-frequency circuits [6].

Currently, advanced bipolar technology is continuously evolving through integration with CMOS processes to form BiCMOS technology with enhanced mixed-signal processing capabilities, providing more comprehensive solutions for relevant applications. Furthermore, the introduction of SiGe technology provides extensive design flexibility for bipolar devices. Through bandgap engineering of the base region, key performance metrics such as frequency, gain, and noise figure can be simultaneously optimized.

3. BiCMOS Technology

BiCMOS technology integrates bipolar devices and CMOS devices onto a single chip, thereby combining the high speed and high drive capability of bipolar devices with the high integration and low power consumption of CMOS devices. It finds extensive application in high-speed, high-performance analog/digital mixed-signal integrated circuits [7]. It can be said that BiCMOS technology is a combination of CMOS technology and additional process modules.

Bipolar junction transistors, known as BJTs are widely used in circuits, particularly in analog circuits. Unlike MOSFETs, bipolar devices are current-control devices. At the same operating current, the transconductance of bipolar devices is significantly higher than that of MOSFETs. This allows it to offer greater gain for the same magnitude of bias current.

Since the current in the bipolar devices is mainly governed by the doping concentration and thickness of the base region, which are process-controlled by diffusion/implantation, thus the precision is better and the device-to-device matching is better than the MOSFET.

As voltage voltage-controlled device, the MOSFET has a simpler drive circuit and lower power consumption in the drive circuit.

Furthermore, due to the simpler structure of the device compared with the bipolar device, the device can obtain a higher integration degree. That is, the complex digital circuit can be built using the BiCMOS process in a smaller package.

It is exactly these two types of devices with different characteristics and advantages that make the BiCMOS process achieve devices with more functions and better performance when integrating them.

According to the type of bipolar device, there are two kinds of BiCMOS processes: the SiBi CMOS process and the SiGe BiCMOS process. As shown in the following figure, SiGe BiCMOS process technology has the advantages of ultra-high speed, low noise and low mismatch. SiGe BiCMOS process technology integrates the SiGe HBT device and the CMOS device on one chip. The two kinds of devices have the characteristics of a large amount of charge carrier types (electron and hole), high carrier velocity, high transconductance and high integration density, respectively. This technology combines the RF performance of SiGe HBTs with the high integration and computational capabilities of CMOS logic circuits, enabling the system to integrate the wireless front-end with digital control and signal processing circuits on a single chip [8,9]. The cross-sectional structure of Si HBT is shown in Figure 3, with its structure and core consisting of the emitter E, base B, and collector C.

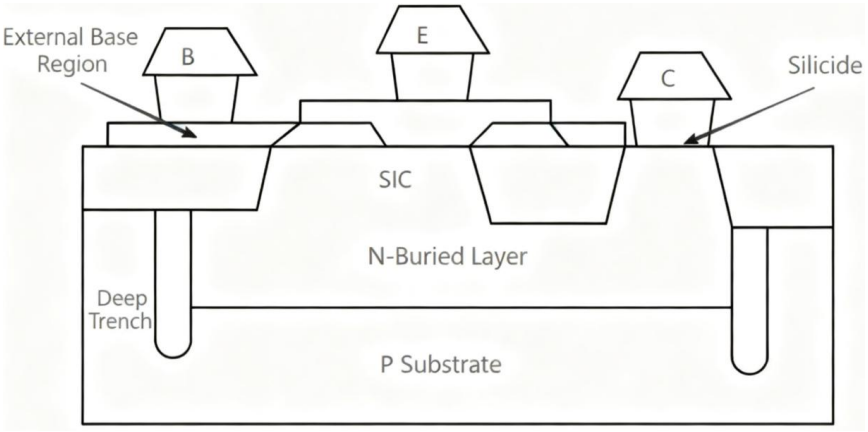
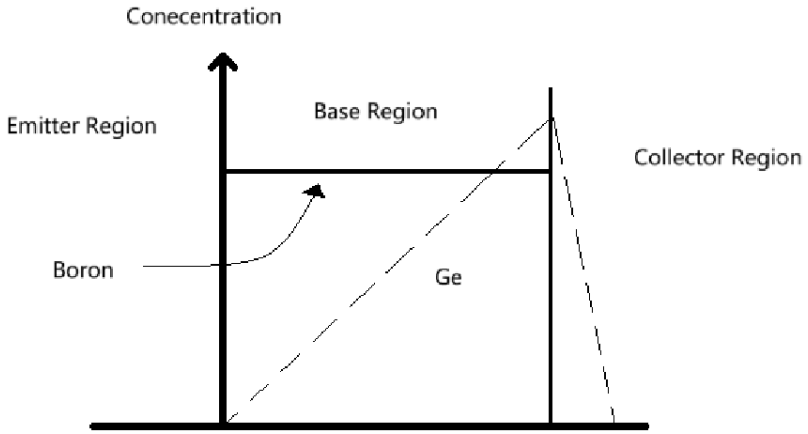
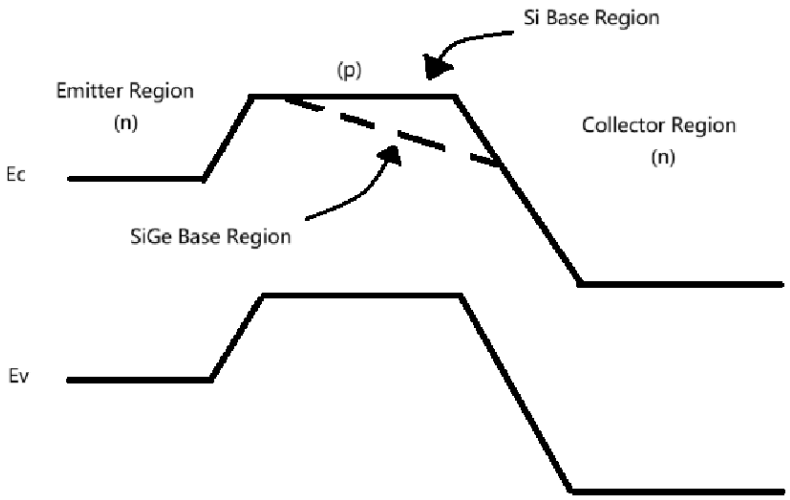


Figure 3. Si HBT Structure

At room temperature, germanium has an energy band gap of approximately 0.67 eV, significantly smaller than silicon's band gap of about 1.12 eV. Consequently, germanium-silicon alloys (SiGe) exhibit a smaller band gap than pure silicon. When germanium is incorporated into the base region of a silicon bipolar transistor, the reduction in the base bandgap width enhances the device's characteristic frequency and current gain characteristics. The principle is shown in Figure 4.



(a) ldeal Distribution Diagram of Boron and Germanium Concentrations in the Base Region of SiGe Base Transistor



(b) Comparison of Energy Band Digrams of Si and SiGe Base Transistors

Figure 4. Comparison of Gradient-Doped SiGe Transistor Designs and Band Structure Characteristics

As shown in Figure 4a, boron is generally doped in the base region to provide a constant carrier concentration, while the molar content of germanium in the germanium-silicon alloy gradually increases from the base region near the emitter to the base region near the collector. As a result, compared to silicon-based bipolar junction transistors (solid line section), the SiGe (dashed line section) base region exhibits a lower conduction band bottom. As shown in Figure 4b, from the base region-emitter boundary to the base region-collector boundary, the band gap width gradually decreases with increasing germanium content, thereby forming an internal electric field directed from the collector toward the emitter. This electric field accelerates the drift velocity of electrons and holes in the base region, thereby increasing the collector current. The base current is determined by the parameters of the emitter junction and therefore does not vary significantly. Consequently, SiGe HBT devices exhibit relatively high current gain and a larger maximum collector current [10].

Currently, SiGe BiCMOS technology continues to advance in two key directions: achieving higher frequency characteristics and enabling monolithic integration with more advanced CMOS processes. Overall, it provides significant improvements to the performance of various electronic components.

4. Non-planar Device Technology

The physical phenomenon known as the short-channel effect occurs when we continuously scale our planar CMOS transistors, and this results in poor device performance that is not ideal for reducing the gate length below 20nm.

For planar CMOS transistors, you can only apply the gate voltage from the top of your channel. When you scale them down to about 20nm, you are basically making your channel very short, such that the source and drain are very close to the gate. The gate primarily controls the current between the source and drain. However, as its contact area diminishes with the shortening of the channel, its control strength weakens, leading to leakage current. This results in electrons flowing from the source to the drain via quantum tunneling even when the CMOS device is in an off state. This will lead to a significant increase in static power consumption and worsen the thermal performance of the device [11]. To suppress nanoscale source-drain leakage currents and enhance gate control over channel carriers, semiconductor technology is gradually shifting toward non-planar MOSFETs. Three-dimensional device structures are gradually replacing traditional two-dimensional planar CMOS devices. A typical example is the FINFET structure [12].

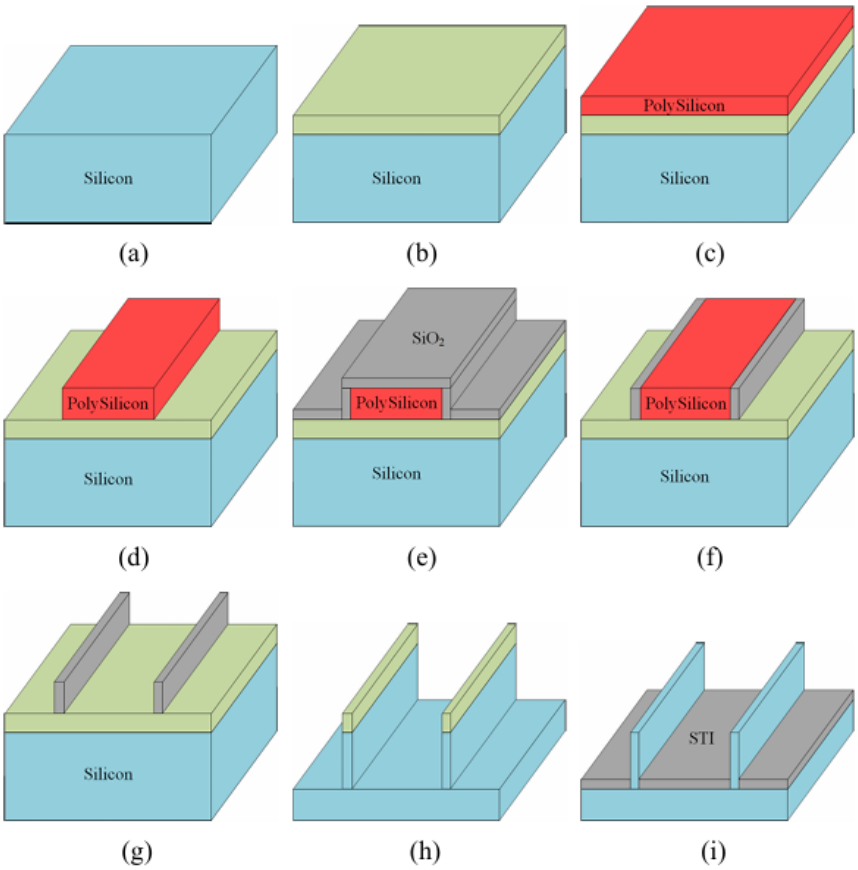


Figure 5. Formation Process of Fin Structures in FinFET Technology [14]

The resulting FinFET structure is shown in Figure 6. As shown in the figure, the protruding channel region in the FinFET structure consists of a very thin silicon channel film. The channel region is enclosed by three-sided gates. By expanding the gate area covering the channel, the electric field interference between the source and drain is reduced. Figure 5 shows the formation process of fin structures in FinFET technology. Enables control of the channel current, thereby lowering the device leakage current and suppressing the short-channel effect [13] [14]. Additionally, due to the enhanced control capability of the gate, the threshold voltage becomes more stable. Since the FinFET structure eliminates the need for highly doped channels, it reduces the effects of impurity ion scattering and enhances carrier mobility, resulting in a significant increase in speed [15].

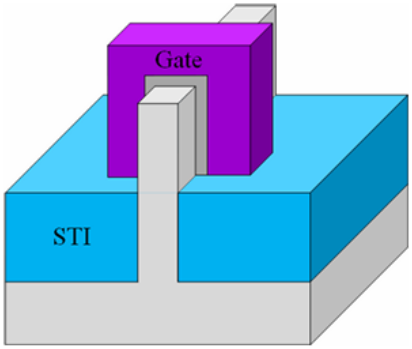


Figure 6. FinFET Structure

In addition to FinFET structures, other non-planar device processes exist, such as GAAFET structures, as shown in Figure 7. In FinFET structures, as dimensions shrink, adjustments to fin height and fin count are required to enhance gate control. However, once the process reaches 5nm, the GAAFET structure with stronger suppression of short-channel effects becomes necessary. The GAAFET structure shows that under this technology, the transistor structure has evolved to feature a gate that is fully enclosed on all four sides, with the channel region passing vertically through the gate. Compared to FinFET, this design further increases the contact area, thereby enhancing its electrostatic control capabilities [16].

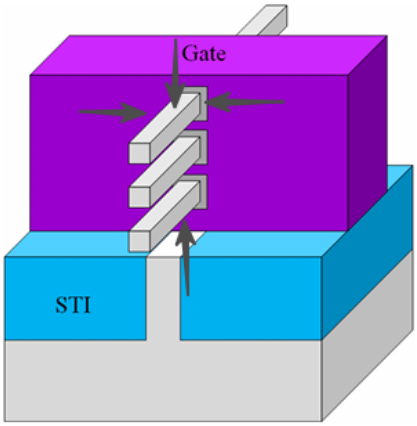


Figure 7. FinFET Structure

There is the NWaFET structure, a process that comprises combining lightly-doped source/ drain regions with heavily doped channel regions, designing epitaxially grown channel regions, and gate control. This process has a great prospect for extending Moore's Law by shrinking the device channel length even more and increasing the integration density. And it makes it possible to make structural improvements that will enhance the characteristics of CMOS devices.

So far in making CMOS devices, the problems they've had with slow response speed, poor drive capability, and problems due to miniaturization have affected the characteristics of the device and integration.

Complementary Bipolar Technology: enables you to fabricate a high-performance PNP transistor that rivals its NPN twin.Improves the bandwidth and output drive capability of the transistor, enabling it to keep pace with high-frequency circuits. BiCMOS technology, such as SiGe HBTs: These devices are integrated with CMOS devices on a single chip to achieve more balanced performance. Non-planar device processes: take advantage of their three-dimensional structure to suppress the short-channel effect, thereby stabilizing the threshold voltage of CMOS devices.

5. Conclusion

As industries increasingly rely on integrated circuits, the demands on CMOS devices continue to grow and become more stringent.

This paper puts forward complementary bipolar technology, which improves the overall device characteristic frequency by changing the structure of PNP transistors to be on par with the NPN transistors. Subsequently, it commences to discuss BiCMOS technology, indicating how SiGe BiCMOS makes the most of the smaller band gap of silicon germanium alloy than pure silicon. This ensures better chip performance when integrated with a CMOS device. Finally, it introduces structures just like FinFET Starting from non-planar process technologies, it details the principles of improvement relative to previous planar CMOS devices, their influence on channel effect, and the resultant improvement in device integration capability.

In summary, this paper analyzes three manufacturing processes—CMOS device fabrication, integration with other devices, and structural enhancements—to elucidate their respective impacts on CMOS device characteristics such as feature frequency and integration density.

Currently, the performance of HBTs fabricated on various BiCMOS processes continues to improve. Structures more advanced than FinFET, such as NWaFET structures, are also emerging. The frequency, power consumption, and integration level of CMOS devices will be further enhanced through advancements in these processes.

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