The Progress of Integrated Circuit Routing Optimization Driven by Artificial Intelligence

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Abstract. As integrated circuit processes move towards nodes below 7nm, the latency of interconnection lines gradually surpasses that of transistors, becoming the core bottleneck restricting the improvement of chip performance. Traditional cabling tools have problems such as large estimation deviations of parasitic parameters, insufficient coordination between layout and cabling, and poor adaptability to special scenarios, which are difficult to meet the requirements of high-density integration. For this reason, artificial intelligence technology has become the key path for wiring optimization. Supervised learning, through incremental parasitic extraction technology, controls parasitic errors within 1%, helping to reduce the delay of 7nm ring oscillators by 10.79% and optimize the efficiency of quantum circuit routing. Reinforcement learning for the collaborative optimization of layout and routing has increased the routing connectivity rate by 8% and shortened the line length by 22%. Meanwhile, the problem of global routing edge overflow is solved through deep reinforcement learning. The heuristic algorithm is adapted to scenarios such as thermal sensitivity of optical networks and dynamic topology of wireless Mesh, achieving a 31.6% reduction in optical power loss and a wireless client connectivity rate of 98%. Experiments have verified the scene advantages of different AI methods, but they still face challenges such as difficult generalization with small samples and complex multi-objective balance at present. In the future, through technologies such as multimodal fusion and generative AI, AI will drive the transformation of integrated circuit design from experience-driven to data-driven precision.

Keywords: Artificial Intelligence, Integrated circuit wiring optimization, Supervised learning, Reinforcement learning, Heuristic algorithm.

1. Introduction

With the advancement of integrated circuit technology to nodes below 7nm, the chip integration has significantly increased, with metal wiring layers reaching 6-10 layers, and the signal delay of interconnection lines has surpassed that of transistors and become a performance bottleneck [1]. The problems of traditional wiring tools are significant. The estimation deviation of parasitic parameters is large. The 3-dB frequency of 3nm DAC drops by 28% due to the neglect of parasitic statistical distribution; The layout and routing are separated; For instance, in a 65nm operational amplifier, the layout is 90% compact, but 30% of the network cannot be connected; The efficiency of a single parasitic extraction of 40nm VCO exceeds 6 hours; More importantly, domestic integrated circuits are prone to failures such as EOS, ESD, and EM due to insufficient redundancy and immature processes, with poor parameters and large quality fluctuations [2]. The parasitic capacitance in the packaging and wiring of neuromorphic circuits leads to the delay of the output spikes of neurons; Although S-Space coding can reduce interference, the parasitic impact needs to be avoided during the wiring stage, making AI the key to breaking through the bottleneck [3].

The current achievements in related fields provide support for AI routing optimization. In routing optimization, supervised learning keeps parasitic errors within 1%, reducing the latency of 7nm ring oscillators by 10.79%. Reinforcement learning improves the routing connectivity rate by 8% and shortens the line length by 22%. Ant colony optimization reduces optical network losses by 31.6%. In the field of fault analysis, microscopic techniques such as OM, SEM, and TEM, electrical techniques like resistance and capacitance testing, and FIB nano-slicing technology can identify problems such as burned bonding wires and clarify the relationship between latch-up, long-term EOS,

and wiring [2]. In the field of neuromorphic circuits, the H-H and Izhikevich models each have their own advantages. The S-Space encoding endows neural information with anti-interference ability and also reveals the influence of parasitic capacitance on output delay [3]. However, the existing achievements have not been integrated and optimized to meet the requirements of reliability and scene adaptation.

This article focuses on AI-driven cabling optimization and sorts out the solutions in existing research to address traditional defects, reliability, and scenario adaptation issues: The first is the supervised learning parasitic sensing scheme proposed by existing research. It correlates wiring parameters with parasitic characteristics through a sensitivity model, optimizes computational efficiency and accuracy by calculating only the modified area and the surrounding capacitance within a specific range, and also combines the neuron circuit modeling method to optimize the relevant wiring to alleviate delay. This scheme has been verified in advanced process circuits and special quantum circuits [3]. The second is the existing research and developed collaborative reinforcement learning method, which designs geometric action models of multiple types of modules, constructs the reward function with "routing connectivity rate - line length", uses DDQN to improve global routing, and combines multi-dimensional failure location technology to verify the inhibitory effect on failures of EOS, EM, etc. [2]. The third is the heuristic cross-scenario adaptation approach explored in existing research. In response to the thermal sensitivity characteristics of optical networks and the connectivity requirements of wireless Mesh networks, corresponding heuristic algorithms are respectively adopted. Meanwhile, by referring to the correlation conclusions between failure modes and cabling, reliability constraints are incorporated into the optimization process [2]. In addition, this paper sorts out and validates the advantages of AI methods, analyzes the challenges, and provides support for advanced nodes and emerging circuit routing.

2. Technical Methods and Practical Progress of Artificial Intelligence-driven Integrated Circuit Routing Optimization

2.1. Supervised learning-driven Parasitic Sensing Routing Optimization

Supervised learning builds a "feature-decision" mapping based on historical data. In the precise modeling of parasitic parameters and the optimization of special circuit routing, the core focus is on data-driven improvement of accuracy and efficiency, and the key achievements are concentrated on the parasitic control of advanced processes and the adaptation of quantum circuit routing. It is necessary to focus on analyzing the performance gain and scene adaptability of key experimental results.

2.1.1. Parasitic sensitive circuit model and incremental extraction technology

In advanced processes (7nm and below), interconnection parasitic parameters (resistance R, capacitance C) have become the dominant factors affecting circuit performance. Traditional full parasitic extraction methods have the dual problems of low efficiency and insufficient accuracy. The single extraction time of the 40nm volt-controlled oscillator (VCO) exceeds 6 hours, and the 3-dB frequency of the 3nm digital-to-analog converter (DAC) drops by 28% due to ignoring the parasitic statistical distribution. All of them are difficult to meet the high-frequency iterative requirements of "modification - verification" in wiring optimization [4]. The core breakthrough of the parasitic sensing optimization framework proposed by the researchers lies in the incremental extraction technology. It only recalculates the parameters within the "maximum coupling capacitance interaction range (MR=1.81μm)" of the modified area and its surroundings, while taking into account the influence of first-order and second-order coupling capacitors to avoid redundancy in full-chip extraction [4].

The experimental results show that the optimization effect of this framework in advanced process scenarios is very significant. In the design of the 7nm 31-stage ring oscillator (RO), the critical path delay was reduced from 9.27ps to 8.27ps, a decrease of 10.79%, and the parasitic error was always

controlled within 1% [4]. In the 40nm VCO design, the center frequency has been optimized from 255GHz to 260GHz, an increase of 1.96%, and the phase noise has also been optimized by 7.1%. More importantly, the total time consumption for the entire wiring optimization was reduced from 4.2 hours using the traditional template method to 0.47 hours (approximately 28 minutes), with an efficiency improvement of 9 times [4]. This performance fully demonstrates that the incremental extraction technology, while ensuring the accuracy of parasitic parameter calculation, significantly addresses the core pain point of "slow calculation" in traditional tools. It is particularly suitable for the high-frequency iterative requirements of wiring optimization under advanced processes, providing efficient support for subsequent design iterations.

2.1.2. Supervised learning enhances the routing transformation of quantum circuits

Quantum circuit routing (QCT) requires adjusting the mapping relationship between logical qubits and physical qubits by inserting SWAP gates to match the connectivity constraints of quantum processors (QPU). However, traditional algorithms have obvious limitations. The simulated annealing heuristic search (SAHS) with a fixed search depth of 2 is difficult to handle deep circuits [5]. Monte Carlo Tree search (MCTS) requires 200 backpropagation iterations, which is too time-consuming [5]. To address this issue, the supervised learning framework achieves optimization through the "offline training - online embedding" model. In the offline stage, shallow quantum circuits (3–5-layer gate structures) are used as training data, and labels are generated using SAHS or MCTS, followed by the training of the policy artificial neural network (ANN) [5]. During the online stage, ANN pruned non-high-quality search branches to enhance search depth and efficiency [5].

The results of the experimental verification highlight the scene advantages of this method in quantum circuit routing. In the Grid 4×4 architecture (16 qubits), SAHS-ANN only retains the SWAP options with the top 30% probability. Even when the search depth is increased from 2 to 5, it still maintains a time efficiency of 7.4 gates/sec. Therefore, compared with the original SAHS's 0.4 gates/sec, the speed is increased by 18 times, while the CNOT gate overhead is reduced by 11%[5]. McS-ann tested 114 sets of real quantum circuits (including quantum Fourier Transform QFT, ADDER, etc.) in two QPU architectures of different scales, IBM Q Tokyo (5 qubit) and Google Sycamore (53 qubit). The SWAP insertion volume is 60% less than that of the industrial-grade tool t > ket, and the fidelity of the quantum circuit always remains above 98% [5]. Even in a large-scale scenario of 53 qubits, ANN can still achieve efficient reasoning through feature compression of qubit coordinates and gate sequences. This performance proves that supervised learning has the dual adaptability of "high precision and high efficiency" in special circuit routing, providing a feasible path for the practical routing of quantum circuits. The optimization effects of supervised learning in the above-mentioned different scenarios can be further clarified through the quantitative comparison of key indicators (see Table 1).

Table 1. Comparison of the Optimization Effects of Supervised Learning in Advanced Processes and Quantum Circuit Routing [4-6]

Scene	Indicator	Results of traditional methods	Supervised learning results	Optimization range
7nm ring Oscillator (RO)	Critical path delay	9.27ps	8.27ps	10.79%
Quantum circuit routing	CNOT gate overhead	Benchmark value	Reduce by 11%	-
Quantum circuit routing	Wiring speed	0.4 gates/sec	7.4 gates/sec	18 times improvement

2.2. Reinforcement learning and Routing Collaborative Optimization Technology

Reinforcement learning regards the routing process as a sequential decision-making problem of "interaction between the agent and the environment", and guides the agent to dynamically balance multiple constraints through a reward function. Its core breakthroughs are concentrated on the collaborative optimization of layout and routing, global routing resource allocation, and the improvement of routing iteration efficiency. It is necessary to focus on comparing the performance gap between the experimental results and traditional methods to analyze its scene advantages.

2.2.1. Collaborative optimization of analog IC layout and routing

In IC design, layout and routing are often handled separately, which can easily lead to the problem that "the layout indicators seem optimal, but the actual routing cannot be achieved." For instance, the layout compactness of a certain 65nm folding common-source common-grid operational amplifier can reach 90%, but during the wiring stage, due to the congestion of the low-level metal, 30% of the network cannot be connected at all [6].

For this issue, the solution approach of reinforcement learning is to directly incorporate routing performance into the layout optimization objective: nine module geometric actions are designed, and then a weighted reward function of "Routing connectivity (RCR) - line length (WL)" is used to guide the agent to learn, ensuring that both high connectivity and short line length are taken into account simultaneously [6].

From the 1060 groups of analog IC cases (each group containing 16 modules and 8 networks, with a layout area utilization rate of 44% to 49%), it can be seen that this method has obvious advantages: compared with the genetic algorithm based on sequence pairs (GA), its line length is shortened by 22% [6]. Meanwhile, compared with the simulated annealing (SA) based on discrete particle swarm, the routing connectivity rate has increased from 80% to 88% [6]. Especially in high-congestion scenarios where the module density is ≥49%, the connectivity rate of traditional methods is mostly below 75%, while it can still maintain 82%. 71% of the cases can also meet the high-performance standard of "RCR≥85% and WL≤5500μm" [6]. This precisely addresses the core issue of "disconnection between layout and routing" under high-density integration, providing a more efficient collaborative approach for the physical design of analog ics [6].

2.2.2. Deep reinforcement learning optimizes global routing

The core OF global routing is to plan the "path backbone" of the network. In the scenario where edge resources are exhausted (the routing capacity at the edge of some grids has been used up), the traditional A algorithm is prone to fall into a local optimum, resulting in an increase in line overflow (OF) [7]. To solve this problem, Deep reinforcement learning adopts the Double Deep Q-Network (DDQN) to improve the "Q value overestimation" problem of traditional DQN. Taking "edge remaining capacity - pin coordinates - wired path" as the environmental state and "selecting adjacent grid nodes as the next path segment" as the action, Design A reward function of "-OF× 10-WL ×1" to prioritize avoiding overflow and conduct 10,000 pre-training (burn-in) times in combination with the path results of Algorithm A to accelerate the convergence of DDQN [7].

In the grid tests of 8×8 and 16×16 scales (each test group contains 20 grids, with 5,000 iterations), DDQN performs best in the "Edge Partial Exhaustion (Type II)" scenario. In an 8×8 grid, the line length (WL) of the traditional algorithm A is 347. DDQN reduces it to 329, with an optimization of 5.2% and no overflow [7]. In A 16×16 grid, the line length of Algorithm A is 1608, and the DDQN drops to 1597, optimizing by 0.7% while still maintaining no overflow [7]. Especially in extreme scenarios where the edge capacity utilization rate exceeds 90%, the overflow rate of the A * algorithm reaches 12%, while DDQN can still maintain zero overflow. This performance is crucial for the scenario of "tight low-level metal resources" in advanced processes, as low-level metals need to connect devices and are prone to congestion. The resource allocation capability of DDQN can effectively prevent wiring failure and ensure the timing convergence of the circuit. The specific optimization data of reinforcement learning in layout-routing collaboration and global routing can be clearly presented through the quantitative comparison in Table 2.

Table 2. Comparison of the optimization effects of reinforcement learning in simulating IC layout - routing collaboration and global routing [6] [7]

Scene	Indicator	Results of traditional methods	Reinforcement learning results	Optimization range
Analog IC layout - routing coordination	Routing Connectivity Rate (RCR)	80%	88%	+8%
Analog IC layout - routing coordination	Line length (WL)	6130.36μm	4781.6μm	-22%
Global routing (16×16 grid)	Line length (WL)	1608	1597	-0.7%
Global routing (edge capacity utilization > 90%)	Overflow rate	12%	0%	-

2.2.3. The deep learning platform accelerates the iterative closed loop of cabling

The routing of analog circuits requires repeated "parameter adjustment - simulation verification". In the traditional process, a single EDA simulation (such as Cadence Spectre) takes several minutes, and the number of iterations for complex circuits (such as integrated voltage regulators IVR) often exceeds 1,000 times, resulting in a design cycle of several weeks [8]. The automated deep learning (ADL) platform significantly reduces the number of simulations by building a "proxy model" for cabling performance. Its core process is divided into three steps. Based on a 3-layer fully connected neural network (with 128-256-128 nodes), input design parameters (such as transistor width-to-length ratio, bias current), and output line-related performance indicators (such as gain, bandwidth, and slew rate SR) [8]. Iterative optimization is achieved by generating candidate routing schemes that meet the constraints through the projected gradient Descent (PGD) optimization model and supplementing the non-compliant schemes with new samples based on the simulation feedback from EDA tools [8].

The experimental results show that the efficiency and accuracy advantages of this platform are both very significant. In the design of 55nm two-stage operational amplifiers, for six performance indicators such as bandwidth and gain, the ADL platform only needs 200 iterations to meet all requirements, while the traditional Bayesian optimization requires 780 iterations [8]. In the 55nm IVR design, the initial sample efficiency of 79% was increased to 88% after 1,000 iterations, and it could also output five sets of optimal solutions with different parameters, which provided designers with a choice space [8]. In addition, the prediction MAPE of the phase margin by the neural network of this platform is only 0.48%, which is much lower than that of the Gaussian process (1.85%) and the random forest (3.04%), and can accurately fit the nonlinear relationship between "design parameters - routing performance" [8].

2.3. Heuristic Intelligent Optimization and Cross-scenario Adaptation

Heuristic algorithms achieve optimization in special scenarios, such as thermal sensitivity of optical networks and dynamic topology of wireless Mesh networks, by simulating the behavior of biological groups or dynamic search strategies. The core lies in finding a balance between "optimization accuracy" and "computational cost", and it is necessary to focus on analyzing the performance gain and constraint adaptation ability in different scenarios.

2.3.1. Ant colony optimized thermal sensing optical network routing

Optical network-on-chip (NoC) relies on silicon micro-resonators (MR) to achieve signal switching. However, MR Is significantly affected by the thermal-optical effect. For every 1℃ change in temperature, the resonant wavelength shifts by 0.1nm. When the offset exceeds 3dB bandwidth, the insertion loss increases sharply, leading to the deterioration of optical power loss [9]. Traditional routing algorithms do not take into account that the temperature distribution is prone to optical signal interruption in the hot spot area at the center of the chip. The ant Colony Optimization (ACO) routing mechanism simulates the behavior of ants "releasing pheromones - following pheromones", using "ants" as control groups to explore paths before routing. The pheromone concentration is negative correlated with the optical power loss of the path. Meanwhile, a "pheromone evaporation" mechanism is designed to prevent the algorithm from falling into local optimum [9]. To address the storage overhead issue in large-scale networks, an approximate ACO (AACO) method was further proposed. By using a linear regression model to replace the pheromone table, the storage requirements were significantly reduced [9].

The experiment took 8×8 grid optical NoC as the test object. The results showed that compared with the West-First routing optical power loss of ACO, it decreased from 15dB to 10.3dB, a reduction of 31.6%, and the throughput increased from 150Gbps to 310Gbps, an increase of 107.3%. The saturation injection rate also increased from 0.15 to 0.25 [9]. When the network scale is expanded to a 16×16 grid, the optical power loss of AACO is only 2.3dB higher than that of ACO, but the storage overhead drops sharply from 5100 entries to 20, a reduction of 99.6% [9]. This performance indicates that ACO can precisely avoid heat-sensitive areas to solve the power loss problem of optical NoC, while AACO further breaks through the "storage bottleneck" of large-scale networks, providing a "low loss - high scalability" adaptation solution for optical NoC cabling.

2.3.2. AI Routing Optimization for Wireless Mesh networks

Wireless Mesh networks (WMNs) are often used in scenarios such as industrial automation and post-disaster communication. They need to address two core challenges: topological dynamic changes caused by node mobility and network congestion resulting from concurrent communication among multiple devices. Traditional routing protocols (such as AODV) rely on periodic routing to discover response lags [10]. The combination of AI and heuristic algorithms forms three types of optimization schemes. Q-learning-feedforward Routing (QFFR) focuses on path selection and learns the mapping of "node signal strength - path selection" through 500 Q-learning iterations. Moth-fire Optimization (MFO) simulates the light attraction behavior of moths to optimize the layout of Mesh routers. The hybrid method combining the Improved Firefly Algorithm (IFA) and Particle Swarm Optimization (PSO) is handled by IFA for global search and PSO for local optimization (inertia weight 0.7) [10].

From the multi-scenario test results, there are significant differences in the adaptability of the three types of schemes. QFFR can increase the packet delivery ratio (PDR) from 80% to 94%, but due to the failure to consider load balancing, the latency increases by 30% in high-congestion scenarios [10]. MFO can increase client coverage from 75% to 95%, but it has a slow convergence speed and a delay of over 100ms during high congestion [10]. The connected client ratio (CCR) of the IFA-PSO hybrid method in the 512-node grid topology WMNs reaches 98%, which is 12% higher than that of QFFR and the delay is controlled within 50ms [10]. This comparison indicates that the hybrid heuristic algorithm can better balance the three major requirements of "coverage - delay - connectivity" and is more suitable for the dynamic scene characteristics of wireless Mesh networks.

2.3.3. Intelligent topology selection for timing violation repair

In ultra-deep sub-micron technology, the influence of routing topology on timing accounts for over 60%. For instance, the RC delay of Manhattan topology is 15% higher than that of non-Manhattan topology. Traditional manual evaluation of topology requires time-consuming simulation of each one and relies on the experience of engineers [11]. The AI-assisted timing repair process is automated in two steps. In the first step, a supervised learning model evaluates multiple candidate topologies

(including Manhattan and non-Manhattan types) generated by global routing and determines the quality of the topology based on features such as "metal layer, RC delay, pin spacing, and overlap with obstacles". The second step is to fix the timing violation for the selected optimal topology by upgrading/degrading the metal layer or adjusting the line width [11].

The experimental results of the four groups of test topologies show that the optimization effect of this process is significant. The RC delay has decreased from 0.000505ps to 0.000327ps, a reduction of 35.2%, and the repair rate of timing violations has reached 90%. For example, the setup violation has been repaired from -0.1ps to + 0.2ps. The hold violation has been fixed from + 0.3ps to + 0.1ps [11]. More importantly, efficiency has been enhanced. The topology assessment and repair work that originally took 2 hours now only takes 48 minutes, and manual workload has been reduced by 60% [10]. In addition, the model's recognition accuracy rate for "non-Manhattan topologies avoiding the M1 layer congestion area" reached 92%, demonstrating its ability to precisely capture the intrinsic relationship between topology and timing, providing efficient automated support for the timing closed loop of ultra-deep sub-micron circuits.

3. Current Challenges and Future Trends

The primary challenge in the current application of artificial intelligence in the optimization of integrated circuit routing is the insufficient generalization ability of the model in small sample scenarios. After the process node advances to 2nm, the cost of routing data annotation increases exponentially. It takes several weeks for a single annotation of a million-gate-level SoC. Moreover, the 2nm and 7nm processes have significant differences in metal layer stacking and parasitic parameters, making it difficult for supervised learning models trained based on 7nm data to adapt to the 2nm process. Especially for special circuits such as radio frequency and quantum, due to their different topological characteristics, the generalization error of existing models has significantly increased. At the same time, the difficulty of balancing multi-objective optimization is prominent. The wiring of integrated circuits needs to take into account timing, power consumption, and area. The conflicts of these requirements are difficult to be dynamically reconciled by existing algorithms. Moreover, the fixed-weight objective functions commonly used in current reinforcement learning and supervised learning cannot be dynamically adjusted according to the design scenarios, resulting in insufficient adaptability. In addition, the "black box" nature of deep learning models leads to a lack of interpretability. Whether it is ANN based on parasitic parameter modeling or GNN with global routing, the decision-making process is not transparent. This not only reduces engineers' trust in AI solutions but also limits their application in high-reliability scenarios such as automotive electronics. Finally, the scalability bottleneck of large-scale systems restricts the development of AI cabling towards billion-gate SoCs. Among them, the improvement of chip integration leads to an exponential growth in the cabling state space. The existing RL and GNN models rely on supercomputing training and inference, making it difficult to deploy to local workstations. In the future, the cross-chip routing of 100-qubit quantum circuits or chiplets will further exacerbate this issue.

In response to these challenges, a full-chain optimization system of "data - efficiency - architecture - trust" can be constructed in the future from four aspects: Multimodal fusion modeling can solve the problems of small samples and generalization at the data level. By integrating the topological information of the circuit network table, the spatial information of the layout diagram, and the parameters of the constraint file, a comprehensive feature representation is constructed, thereby reducing the reliance on a single data point and simultaneously enhancing the AI's global understanding of complex circuits. Generative AI will revolutionize the traditional "net-to-network optimization" model. By leveraging GAN and diffusion models, it can directly output full-chip routing solutions without the need for step-by-step optimization to shorten time. Moreover, it can adapt to different processes through "style transfer". For emerging architectures such as Chiplet 3D stacking and computing-in-memory, it is necessary to develop dedicated AI adaptation technologies. In 3D stacking, optimize the TSV distribution to reduce cross-layer parasitism, and in computing-in-

memory, prioritize the selection of shorter paths to reduce power consumption by learning the correlation between data transfer paths and power consumption. Finally, integrate explainable AI (XAI) to address the "black box" trust issue. By leveraging the attention mechanism to visualize decision-making basis, it helps engineers quickly identify problems, promoting the transformation of AI cabling from an "auxiliary tool" to a "core design approach".

4. Conclusion

This article focuses on the research of artificial intelligence-driven integrated circuit routing optimization. Through three types of AI technologies, it specifically addresses the core pain points of traditional routing tools and achieves remarkable results: Supervised learning, relying on incremental parasitic extraction technology, keeps the parasitic error within 1%, reducing the critical path delay of the 7nm ring oscillator by 10.79%, and simultaneously increases the quantum circuit routing efficiency by 18 times, thus solving the problems of parasitic inaccuracy in advanced processes and low efficiency in special circuit routing. Reinforcement learning achieves collaborative optimization of layout and routing, increasing the routing connectivity rate by 8%, shortening the line length by 22%, and solving the global routing edge overflow problem through deep reinforcement learning, thus breaking the "optimization disconnection" predicament caused by the separation of traditional layout and routing. The heuristic algorithm precisely ADAPTS to cross-scenario requirements, reducing power loss by 31.6% in optical network-on-chip and achieving a client connectivity rate of 98% in wireless Mesh networks, solving the wiring adaptation problem under thermal sensitivity and dynamic topologies.

The core value of these achievements lies in providing efficient solutions for the routing of advanced processes below 7nm and complex circuits such as quantum and optical NoC. They not only make up for the shortcomings of traditional tools, such as large parasitic estimation deviations, low iteration efficiency, and poor scene adaptability, but also promote the transformation of integrated circuit design from the traditional model that relies on engineers' experience. The transformation to a data-driven precision model lays the foundation for the performance improvement and reliability guarantee of high-density integrated chips.

In the future, with the development of multimodal fusion modeling, generative AI, adaptation of emerging architectures (Chiplet, 3D stacking), and explainable AI technologies, AI routing optimization will further break through the bottlenecks of small sample generalization, large-scale expansion, and "black box" trust, providing more efficient support for the routing requirements of billion-gate SoCs and hundred-qubit quantum circuits, and continuously promoting the evolution of EDA technology towards a smarter and more reliable direction.

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