Impacts and Limitation of New Generation Semiconductor Materials on Energy Efficiency and Frequency: Application for CPU and FPGA Technologies

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Abstract. The silicon-based complementary metal–oxide–semiconductor (CMOS) technology has been making progress in computing performance for the past decades. The modern central processing unit (CPU) and field-programmable gate array (FPGA) architectures are constrained by fundamental limitations caused by material properties, such as short-channel effects, latency in interconnections, and the distribution of heat density. As the operating frequency reaching to the 3–5 GHz and the thermal dissipation reach the physical maximum, the innovations of material become essential for future performance improvements. This paper reviews and analyzes the new-generation semiconductor materials, wide band-gap gallium nitride (GaN), ultra-wide band-gap (UWBG) gallium oxide (Ga_2O_3), and molybdenum disulfide (MoS_2), which influence the energy efficiency, switching behavior, and design for CPUs and FPGAs. The wide band-gap materials provide outperformance breakdown fields, lower switching loss, and high-temperature stability, which directly improve the FPGAs' voltage regulation and responses. The MoS_2 offers thinner channels, electrostatic gate control, and the back-end-of-line (BEOL) integration compatibility, providing a design direction for further ultra-scale single-chip FPGAs.

Keywords: Semiconductor materials, Wide band-gap, FPGA architecture, Energy efficiency, Frequency scaling.

1. Introduction

In the past century, human computing power has experienced not only qualitative but also quantitative leaps compared to the early stages. The development and evolution of semiconductor technology drive this significant change and advancement. Starting from reducing the scale of processes and fabrication from micrometer-level devices to nanometer-scale, from single-core to multi-core architectures. The modern chip manufacturing process follows Moore's Law and Dennard scaling, which relies on the improvement of the transistor density to improve performance on silicon-based materials. The representative computing architectures, CPUs and FPGAs, serve as general-purpose computing and reconfigurable computing, playing core roles in data centers, artificial intelligence, high-performance computing, and embedded systems. However, as the design and manufacture enter the 7nm, 5nm, and even 3nm era, the traditional silicon-based CMOS technology faces a physical bottleneck. The size of the transistors is approaching the critical quantum limit; therefore, the short-channel effects and increased power consumption limitations become the key challenges for future performance improvements.

Over the past few years, the growth and development of CPU clock speeds have slowed significantly. The mainstream commercial CPUs were limited to a range of 3–5 GHz, and the nonlinear power consumption growth, along with the rapid increase in heat density, became significant factors limiting frequency development. Different from the architectural or software, the optimizations in frequency leads to dynamic power consumption increase approximately proportional to the square of the frequency and voltage ($P_{dynamic} \propto V^2 f$), which means every small increase in frequency come with a significant increase in thermal load. With the dense stacking of transistors, the heat flux density of modern high-performance chips has reached the dissipation rate limit, making heat dissipation and material heat transfer capabilities a "thermal wall" that restricts further frequency increases. This also represents solely relying on the silicon-based materials, and traditional packaging

and heat dissipation methods are no longer sufficient to meet the needs of the future demands of high-performance computing.

Under this background, materials innovation has become the key method or approach to break the performance bottlenecks. Apart from the more advanced gate engineering and new three-dimensional transistor structures, an unexpected semiconductor material has entered the view of researchers, the third-generation semiconductor materials, such as GaN and SiC, these materials have a higher band-gap, a higher breakdown electric field, and better thermal stability. Compared with traditional semiconductors, they have significantly reduced losses, in return improving energy efficiency in power electronics, high-frequency RF systems, and such areas. In the meantime, diamond films, graphene thermal interface materials, and other high thermal conductivity materials are under testing and introduced to the packaging process to improve on-chip heat dissipation capabilities.

Thus, the field of computing research is in the process of transitioning from process-driven to materials-driven. This paper will begin with the characteristics of semiconductor materials and the requirements of chip architecture, analyze the influence of materials engineering on the energy efficiency and frequency performance of CPUs and FPGAs, and explore the advanced materials such as GaN in current applications and the potential of advanced materials, then look forward to the next-generation materials and packaging technologies in the future for high-performance computing. With an analysis of relationships between materials, architecture, and thermal perspective, this paper aims to provide a systematic overview and reflection on the future evolution path for computation chips.

2. Fundamental Background

2.1. FPGA Architecture and Material Limitations

FPGA is a type of device that allows dynamic configuration of hardware logic through programmable logic cells and reconfigurable interconnects based on scenarios and functions. Different from the general-purpose CPUs, FPGAs implement computations directly in hardware using a parallel architecture. The basic structure of the modern FPGA, including lookup tables (LUTs), configurable logic blocks (CLBs), on-chip memory, DSP modules, and a large number of programmable connection switches, buttons to control functions, and, of course, the wiring and inner connection components. Compared to traditional CPUs, the FPGA provides high parallelism and flexibility

This reconfigurable structure allows FPGAs to optimize data-paths for specific workloads to achieve massive parallelism, minimize latency, and increase energy efficiency. Instead of executing instructions within a fixed pipeline, the customized logic structures can significantly reduce memory access limitations and power consumption.

A study shows that approximately 60%–80% of the overall latency in an FPGA is coming from the interconnect paths rather than the logic cells. Thus, interconnected resistance, capacitance, and other dielectric constants by material are key factors affecting its clock frequency. They far outweigh the latency caused by the gate; further shrinking in size to the sub-micron scale, the wire propagation delay is far slower than the transistor switching speed, resulting in the interconnect accounting for the majority of time consumption and constraining the clock frequency in modern programmable fabrics [1].

As Hauck and DeHon noted, the reconfigurable computing paradigm in FPGAs allows the hardware to “retarget to different tasks on a sub-second timescale,” which links the gap between ASIC-level performance and CPU-level programmability [2].

2.2. Semiconductor Material Parameters

The materials for semiconductor are fundamental to determine the electrical and thermal properties. Physical properties such as band-gap width (E_g), electron mobility (μ), dielectric constant for material

(ε_r) and the thermal conductivity (k) directly impact the switching speed, leakage current, power density, and reliability these key factors of transistors [3].

The traditional silicon-based CMOS processes have made silicon the mainstream material for integrated circuits, due to its mature manufacturing procedure, excellent crystal growth quality, and lower cost. However, as the size of products and devices reduces significantly to 7 nm or even below 5 nm, the silicon MOSFET begins to face short-channel effects, an increase in leakage current, and more difficulty in suppressing parasitic capacitance. Most importantly, this also poses a heat dissipation problem.

From a device physics perspective, material properties directly influence the system's energy efficiency boundary.

Band-gap width (E_g) is used to determine the intrinsic carrier concentration, the energy required for a transition from the valence band to the conduction band ($n_i \approx e^{-\frac{E_g}{2kT}}$). Compared to silicon, materials with a wider band-gap exhibit significantly lower leakage under high temperatures and pressures, which improves reliability and efficiency [4].

Electron mobility (μ) is the rate at which charge carriers move within the material. The higher mobility represent transistors can drive a larger current with the same gate voltage or capacitance, which leads to shorter channel delays and higher switching speeds. This is significantly important for frequency improvement in logic and FPGAs. In conclusion, the mobility of the carrier results in lower energy consumption per unit switching and minimizes the delays, thus reducing chip frequency or reducing power consumption [5].

Electrical breakdown (E_c) is the maximum electric field strength a material can withstand. With higher electrical breakdown, the design for the drift region can be made thinner within the required voltage region, thereby reducing drift resistance and conduction losses. This also means that a device or component can operate and withstand higher voltages, thereby satisfying the requirements of more demanding environments. The system impact for higher breakdown voltage devices is lower conduction losses, which leads to an increase in operating frequency, and improves and minimizes device size, leading to higher power density [6].

Dielectric constant (ε_r) has an effect on the capacitance of the transistor's gate and channel. Larger capacitance results in increased energy consumption during the switching process, indicating higher energy losses. Materials with a lower dielectric constant have an advantage in reducing parasitic capacitance, minimizing latency, and reducing dynamic power consumption. Inside the high-frequency logic or FPGAs, interconnects and switches are across the design, and the reduction in parasitic capacitance will result in a significantly increased clock frequency [3].

Thermal conductivity (k), this property determines the ability of a material to dissipate heat through the crystal structure and interfaces. Materials with high thermal conductivity can quickly dissipate heat from devices, reducing the rate of increase in thermal resistance and thereby decreasing the junction temperature. Thereby, slow down the rate of increased resistance, mobility reduction, and decrease in reliability of the devices, which are the key to high-frequency and high-power density operations [7].

Based on these properties, the third-generation wide band-gap semiconductors such as GaN and SiC have significant advantages compared to silicon-based semiconductors in high-voltage, high-temperature, and high-frequency applications in a variety of fields. They have been quickly applied in consumer fast charging, inverters for electric vehicles, power supplies for data centers, and modern RF systems for 5G communications.

3. Next Generation Semiconductor Materials Analysis and Review

3.1. GaN: Material Properties, Device Physics and FPGA and CPU Implication

Gallium nitride is a typical wide-band-gap semiconductor with unique crystalline structures of the wurtzite hexagonal phase. This wurtzite lattice crystal structure lacks inversion symmetry along the

c-axis, leading to strong spontaneous polarization and additional piezoelectric polarization. The polarization side effects within the material are the fundamental differences between gallium nitride and conventional semiconductors such as silicon, which directly facilitated the high-density conduction mechanisms observed in the $AlGaN$ or GaN heterostructure.

Gallium nitride is the III–V group material semiconductor with a common wurtzite crystal structure. As shown in Figure 1, the intrinsic band-gap is approximately 3.4 eV, within the range of wide band-gap semiconductors; the critical breakdown electric field is 3 to $3.5MV/cm$. These unique properties provide gallium nitride with a fundamental physical foundation for high-temperature, high-voltage, and high-frequency operation.

The primary gallium nitride device has different mechanisms in both physics and device areas due to the $AlGaN$ and GaN HEMT architecture. At the heterogeneous junction of $AlGaN$ and GaN, two different polarizations, spontaneous and piezoelectric, induce a two-dimensional electron gas, resulting in a yield $1 * 10^{13}$ level of carriers per square centimeter without doping; this leads to high transconductance and high current density of devices. Ambacher et al. established the theoretical and experimental foundation and concept for polarization-induced 2DEG [8]. In the practical engineering application, the GaN devices are categorized into two separated model, the depletion-mode and enhancement-mode. Gate-injection transistors, p-gate devices formed by GaN material stacking, and other techniques have been developed to achieve "normally-off" operation. Especially the Uemoto et al. using $p - AlGaN$ hole injection to modulate the channel conductivity in gate-injection transistors concept has significantly increased the safe turn-off, allowing the device to stably and controllably pause the conducting electricity to avoid voltage/current spikes or breakdown, and maintain conductivity [9].

Although the logic transistors within CPUs or FPGAs are made by GaN, but the material advantage significantly influence the power supply performance. The wider band-gap, high electron mobility, and low parasitic capacitance of GaN allow to to operate with extremely low energy consumption at megahertz level alternating frequency, which can achieve the difficulties face with silicon MOSFETs, the high-bandwidth voltage regulators (VRMs) and point-of-load converters (PoLs).

For high-density FPGAs, the reconfiguration and computation will create rapid load current changes. The GaN power stages can significantly reduce control loop delays and minimize the voltage transient deviation. The lower level in gate charge and output capacitance will lead to faster turn-on and turn-off, and the smaller reverse recovery charge will significantly reduce dead-time losses. All these characteristics of GaN-based devices will stabilize the output voltages, restrain overshoot, and thereby improve the FPGAs' timing sequence and maximum operating frequency.

At the board level, high switched frequencies will also improve the magnetic components, such as inductors, transformers, and capacitors, and reduce the size of these components. With this size-wise improvement, the VRMs can be placed closer to the FPGA package. This close-up packaging power supply structure reduces parasitic inductance in the PDN, thereby improving both electrical and thermal efficiency. Research suggested that GaN-based 48 V to 1 V converters can achieve peak efficiencies exceeding 95%, while reducing size by over 40%, resulting in higher power density and lower heat dissipation requirements [10, 11].

3.2. Ga_2O_3: Material Properties, Device Physics and High Voltage Implication

The other semiconductor material that has attracted significant attention recently is Ga_2O_3, an emerging UWBG semiconductor material. The β-phase Ga_2O_3 is the most thermodynamically stable form, which has approximately 4.8–5.0 eV direct band-gap significantly wider than that of gallium nitride (GaN, 3.4 eV) and based on calculation, over 8 MV/cm breakdown electric field, which is about 2 times higher compare to the GaN in the previous parts [12, 13]. The unusually large field strength directly represents Baliga's figure of merit (BFOM), which defines the efficiency limits of power switching devices. Studies such as Higashiwaki et al. and Tsao et al. demonstrate that Ga_2O_3-based devices can potentially achieve BFOM values that an order of magnitude higher than

those of SiC MOSFETs under the same blocking-voltage conditions [12, 14]. These intrinsic properties make Ga_2O3 a very promising material for future high-voltage and high-power electronic devices.

One of the unique advantages of the Ga_2O_3 is the compatibility of its growth under meting conditions, including Czochralski, float-zone, and edge-defined film-fed growth (EFG), with these techniques, the large-area, high-quality single-crystal fabrication of Ga_2O_3 costs significantly less compared to GaN and SiC [13, 15]. Different from GaN and SiC, which require expensive vapor-phase or sublimation growing processes, Ga_2O_3 can be produced directly from the melt and allows the diameter of the commercial wafers to exceed 4 to 6 inches. The study of Yamaguchi et al. suggests the $\beta - Ga_2O_3$ grower from the melt has low defect densities and high resistivity, which is extremely suitable for high-voltage device fabrication [15]. This phenomenon significantly demonstrates and improves the scalability of ultra-wide band-gap (UWBG) power electronics.

In the applications of the device, the Ga_2O_3 showed huge potential in unipolar device structures such as Schottky barrier diodes (Metal structure diodes), FETs, and MOSFETs. All of these are experienced by Sasaki et al. The lateral structure device of Ga_2O_3 MOSFETs has breakdown voltages over 8 kV, while the vertical structure device shows a higher than 10 kV blocking capability and with a lower forward-voltage drop [16]. These statistics and analyses highlight the intrinsic advantage of Ga_2O_3 material used for high-voltage switching devices. More importantly, the unique structure grown by Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapor Deposition (MOCVD) shows a low interface trap density and high electron mobility, from specific material properties to support low-loss conductivity and fast switching [12, 16, 17].

Despite the many advantages listed above, Ga_2O_3 material also faced several physical limitations. To begin with, the thermal conductivity is significantly lower compare to GaN, 10–27 W/m·K compare to 230 W/m·K, which leads to expected challenges in heat dissipation during high-current operation [14, 18]. Additionally, achieving stable p-type doping in Ga_2O_3 is one of the most critical limitations and challenges in the material system. Several studies shows that conventional acceptor dopants such as magnesium and zinc will introduce deeper acceptor levels, typically with a range of 0.5–1.1 eV above the maximum value of the valence band, which will make the thermal activation of holes quite impossible at room temperature [12, 14, 19]. Even with the acceptor impurities introduced into the material during the growth process, the first principle in the Van de Walle team study suggests that Ga_2O_3 also exhibits a strong self-compensation behavior, a donor-like defect will form spontaneously and neutralize the intended acceptor states [14, 19, 20]. This impact will severely limit the concentration of the holes and prevent the formation of a functional p-type conduction channel.

With these intrinsic physical constraints and limitations, Ga_2O_3 is considered a material system fundamentally limited to unipolar device architectures. Different from GaN, Ga_2O_3 will not be able to form functional p–n junctions or bipolar devices. This limitation not only restricts the flexibility of device design but also presents challenges for advanced circuits. The system application level for Ga_2O_3 is to leverage its high-voltage handling capability and introduce this material into ultra-high-voltage rectifiers, satellite power electronics, and fields that require high breakdown strength, while also achieving cost efficiency.

3.3. MoS_2: Material Properties, Device Physics and Potential for Future FPGAs.

Different from the wide-band-gap materials such as GaN and Ga_2O_3, MoS_2 is one of the most studied transition metals dichalcogenides (TMDs). Compared to the wide-band-gap materials, such as GaN and Ga_2O_3, which are under three-dimensional covalent crystal structures with significant band gaps and high breakdown fields designated for high-power electronics, the MoS_2 is an atomic-level two-dimensional (2D) semiconductor, which is held together by van der Waals forces without surface bounding [21]. These structural differences confer MoS_2 several unique physical properties, which distinguish it from traditional WBG semiconductors.

First of all, the fundamental difference in band-gap, unlike the GaN, band-gap energy is approximately 3.4 eV or the Ga_2O_3 band-gap energy is around 4.8–5.0 eV, who have tremendous

advantage in high-voltage operation, the single layer MoS_2 has direct band-gap around 1.8 eV, which exhibit a power gate electrostatic control even with nanometer-level thickness [21]. Due to the channel thickness of MoS_2 being limited to a single molecular layer, approximately 0.65 nm, this material exhibits a significant performance in suppressing short-channel effects compared to ultra-thin silicon, GaN, or Ga_2O_3. With the support from Desai et al.'s studies, MoS_2 can maintain channel integrity even with a gate length of only 1nm, which is impossible for 3D semiconductors due to their size limitations, resulting in source or drain tunneling and degraded electrostatics [22].

This ability to maintain control of the gate at atomic thickness makes MoS_2 particularly suitable for future logic high-density embedded FPGA. The advanced FPGAs become deeply reliant on scaled FinFETs or nano-level sheet transistors, but their performance is strictly limited by electrostatic degradation, loss in mobility, and short-channel effects. Different from the MoS_2, the wide band-gap materials like GaN or Ga_2O_3 can not form complementary logic due to the band-gap characteristics of poor hole mobility and strong polarization fields within. On the other hand, the MoS_2 is capable of constructing logic devices with high frequency ratios, reduced leakage voltage, and high gate controllability, which is an ideal material candidate for FPGA core logic in below 5nm and future generations [23, 24].

Another unique characteristic is the absence of surface bounding, which minimizes interface scattering and forms extremely clean and pure semiconductor dielectric interfaces. This is essential for stabilizing the threshold voltages and low leakage power in FPGA logic modules. Unlike GaN and Ga_2O_3, these wide-band-gap materials with surface or interface traps significantly influence the threshold behavior, and their impact also alters and complicates their application in digital circuits.

The flat 2-D surface of MoS_2 also allows it to be assembled layer by layer through a van der Waals stacking process, and since MoS_2 does not rely on lattice matching, it can be transferred or directly grown on the top of completed CMOS wafers without causing dislocations or other defects [25, 26]. More importantly, the MoS_2 material can be processed at temperatures below 400 °C, which is within the range of BEOL fabrication. The logic devices based on MoS_2 material can be fabricated after the metal interconnect stacking, which can significantly improve integration density and reduce connection delay, a feature that high-temperature semiconductors, such as GaN or Ga_2O_3, cannot achieve.

This possible route and compatibility of BEOL introduce a brand-new architectural design for future FPGAs, which directly stacks the MoS_2 logic layers above the switch boxes and the configuration SRAM blocks. This can increase logic density without additional lateral direction scaling, and physically place the transistors closer to the interconnect layers, thereby shortening the wire length and reducing the routing delay. Due to the modern limitations of FPGAs, which are interconnect delay and wire energy losses, therefore, the vertical stacking of MoS_2 layers can improve the overall operating frequency and lead to higher computational throughput [25-27].

To compare with the wide band-gap semiconductors' material, 2D materials such as MoS_2 can be integrated in the vertical direction, so the logic units, lookup tables, and local routing switches of FPGAs can be distributed into multiple layers across the design, resulting in reduced routing layers and providing new possibilities for new type FPGA architectures. This optimism in design is not limited to a single silicon plane, but across 3D space.

In summary, MoS_2, from a material aspect, not only provides an alternative transistor channel but also offers a different materials platform, which directly targets power density, size scaling, and connection within the design. Different from wide band-gap materials, which have an advantage in high-power switching and high-voltage operation, the MoS_2 has the advantage of a combination of atomic-level thickness and compatibility with BEOL, becoming a potential material for future high-density, low-power consumption FPGA systems.

4. Conclusion

With the silicon-based CMOS technology entering the sub-5 nm regime, the transistor is approaching its fundamental physical limits. Short-channel effects, escalating thermal densities, and other challenges are limiting the frequency and energy efficiency of modern CPUs and FPGAs. Under this context, the innovation in the semiconductor material area becomes essential for the next stage of computing performance evolution.

The paper examined three different next generation semiconductor materials, GaN, Ga_2O_3 ,and MoS_2, describe and analysis the distinct physical advantages and implications in systems. GaN exhibits a balanced improvement in breakdown field, electron mobility, and switching energy losses, which enables a high-efficiency power transfer module and directly enhances the FPGA's transient performance and maximum operating frequency. The ultra wide band-gap material Ga_2O_3 took further improvement in these areas, with never seen before breakdown strength and low-cost growth in the melt, despite the limited thermal conductivity and the absence of p-type doping, this material is high suitability for future high-voltage power electronics. Compare to these two materials, the two-dimensional semiconductor MoS_2 representing a different type of design, the atomic-level thickness and BEOL processing provide unique vertically integrated FPGA logic layers, which bypass the current latency bottleneck and other restrictions.

In conclusion, these materials indicate that high-performance computing in the future will increasingly rely on material and architectural design rather than scaling device size. As the requirements of computing workloads become increasingly complex and energy restrictions become more severe, advanced semiconductor materials will predominantly define the boundaries and limitations of CPU and FPGA performance, and with new designs, achieve performance beyond the limitations of silicon.

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