Design of Capacitor-Less Low-Dropout (LDO) Voltage Regulator

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Abstract. With the rapid proliferation of portable electronic devices and growing demands for energy efficiency, the critical role of low-dropout linear regulators (LDOs) in power management has become increasingly evident. This paper focuses on the design of capacitor-less LDO integrated circuits, providing a comprehensive and systematic analysis of existing solutions. The fundamental operating principle of LDO regulators is introduced, followed by a review of the technological evolution and development background of key research topics such as capacitor-free LDOs, high power supply rejection ratio (PSRR) LDOs, and fully integrated on-chip LDOs. To overcome the limitations of conventional capacitor-less approaches—including poor transient response, limited loop stability, and high power consumption—two mainstream design architectures for capacitor-less LDOs are analyzed in depth. The core innovations, resolved technical challenges, and resulting performance advantages of each scheme are elucidated. Furthermore, limitations and drawbacks of these designs in critical aspects such as noise susceptibility, structural complexity, and power transistor performance are critically assessed. Finally, based on the identified shortcomings, prospective optimization directions and potential technological pathways for future capacitor-less LDO designs are proposed.

Keywords: Low-dropout linear regulators, Capacitor-less LDO, Loop stability, Transient response.

1. Introduction

In contemporary society, electronic devices have permeated all aspects of daily life. Portable electronic products such as smartphones, tablet computers, and laptops play an indispensable role in people's routines. For these devices, the performance of power management integrated circuits (PMICs) critically determines their overall functionality. Given the requirements for features such as instantaneous calibration, output state self-checking capability, as well as low dropout voltage, low quiescent current, low system cost, and design simplicity in voltage regulation, the low-dropout linear regulator (LDO) has undoubtedly emerged as the most suitable solution [1, 2].

As energy efficiency becomes a globally emphasized priority, increasing attention is being devoted to the field of power management. Among the market share distribution of power management ICs, LDO regulators account for the largest proportion. Key technological advancements—such as ultra-low quiescent current (IQ) with dynamic frequency adjustment [3], and digitally-assisted analog techniques for enhanced transient response—exemplify the ongoing innovations in this area. This paper aims to provide an in-depth analysis of existing LDO architectures and current research trends, with a dedicated focus on capacitor-less LDO designs and their implementation strategies.

2. Relevant Work

2.1. Theoretical Fundamentals of LDO Integrated Circuits

The LDO operates based on a negative feedback mechanism, which stabilizes the output voltage by adjusting the input to the error amplifier. Figure 1 illustrates its basic structure, which primarily consists of a reference circuit, an error amplifier (EAMP), auxiliary circuits, and a pass device. The core components—the error amplifier and the pass device—form a closed-loop negative feedback system through a feedback resistor network, thereby enabling the LDO to maintain a stable output voltage via internal negative feedback [4]. The reference circuit, typically implemented using a

bandgap voltage reference generator, supplies reference voltage and current to the LDO chip. The auxiliary circuits are designed to support functions such as auto power-on, over-current protection, and thermal shutdown.

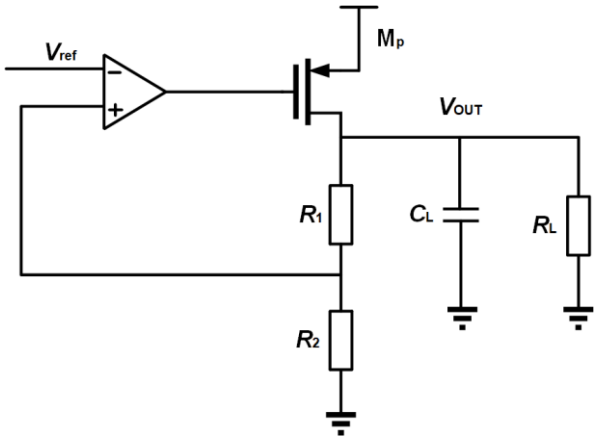


Figure 1. Block Diagram of a Traditional LDO Structure

2.2. Key Research Focus Areas in LDO Integrated Circuits

With the advancement of System-on-Chip (SoC) and consumer electronics such as smartphones and laptops, the design focus of LDO integrated circuits has shifted from traditional metrics like low power consumption and high load current capability to high power supply rejection (PSR) and fully integrated on-chip implementations [5].

2.2.1 Capacitor-Less LDO Integrated Circuits

Traditional LDO integrated circuits require an external load capacitor C at the output to suppress output voltage overshoot and stabilize the internal control loop. Owing to their low-noise, low-ripple, and EMI-free characteristics, LDOs are often employed within System-on-Chip (SoC) or mixed-signal integrated circuits—such as those integrating analog-to-digital (ADC) and digital-to-analog (DAC) converters—to supply noise-sensitive submodules.

However, in such applications, if an external load capacitor is necessary, the SoC must dedicate additional pins to connect to this external component. This not only occupies valuable die and printed circuit board (PCB) area but also increases overall system cost. When multiple LDO modules are integrated into a single SoC to power different functional blocks, each requiring its own dedicated pin and external capacitor, the system cost increases significantly [6].

As a result, capacitor-less LDO architectures have emerged as a major research focus in recent years.

2.2.2 High Power Supply Rejection LDO Integrated Circuits

To enable devices to transmit more information within shorter time frames, narrower bandwidths, and with lower energy consumption, it is imperative for integrated circuits not only to operate at higher frequencies but also to achieve a higher signal-to-noise ratio (SNR). Consequently, suppressing power supply noise across elevated frequency ranges has become a critical challenge for LDO integrated circuits designed to power analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) [7].

2.2.3 Novel Frequency Compensation Schemes

Against the backdrop where capacitor-less design and high power supply rejection (PSR) have become major research focuses in LDO regulators, conventional frequency compensation schemes are no longer compatible with emerging LDO architectures. Consequently, novel frequency compensation strategies are required to ensure loop stability under the constraints of eliminating external load capacitors and achieving high power supply noise rejection [8].

2.2.4 Optimization of LDO Transient Response

The transient response of an LDO refers to the process wherein the output voltage changes in response to sudden variations in load current or supply voltage, and the regulator restores stability through linear negative feedback. Key performance metrics include overshoot voltage and recovery time. Excessive overshoot voltage may cause breakdown of MOS transistors in certain digital circuits, while recovery time determines how long it takes for the output to restabilize. The transient response is influenced by both the small-signal characteristics of the control loop and the large-signal behavior of the amplifier's charging and discharging of the load capacitance. Therefore, coordinating the trade-offs among error amplifier bandwidth, slew rate, and power consumption, along with incorporating auxiliary circuits to enhance large-signal performance, has become a major research focus in contemporary LDO design.

3. Design Schemes for Capacitor-Less LDO Integrated Circuits

3.1. Design of Low-Quiescent-Current,High-Transient-Response Capacitor-Less LDO

To address the limitations of conventional capacitor-less LDOs, such as inadequate transient response and poor loop stability, Tian Lin et al. proposed a low-quiescent-current, high-transient-response capacitor-less LDO based on SMIC 0.18μm BCD process technology [9].

The key innovation of this design lies in a transconductance enhancement technique applied to the error amplifier, which achieves higher loop gain and unity-gain bandwidth while maintaining low quiescent current. The size of the pass transistor was appropriately reduced to improve transient performance. Active feedback was introduced to increase the secondary pole frequency while avoiding the generation of a right-half-plane zero, thereby enhancing loop stability. Furthermore, based on this active feedback structure, a small capacitor was connected in parallel with the feedback resistor to improve stability under light-load conditions. Figure 2 shows the complete circuit of the proposed LDO scheme.

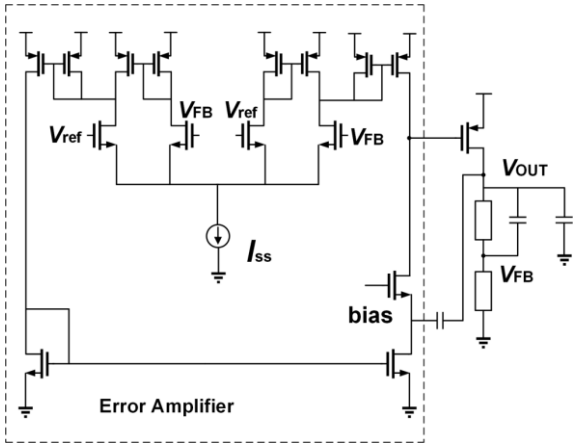


Figure 2. Complete Circuit of the Proposed LDO Scheme

In this design, the error amplifier primarily consists of a main transconductance stage, an auxiliary transconductance stage enhanced by a transconductance boosting technique, and current mirrors. Compared to conventional error amplifiers, the proposed architecture employs a transconductance enhancement strategy, which effectively increases the input transconductance of the error amplifier under low quiescent current conditions. Thereby, it improves the overall loop's unity-gain bandwidth and accelerates the system response, resulting in significantly enhanced transient performance.

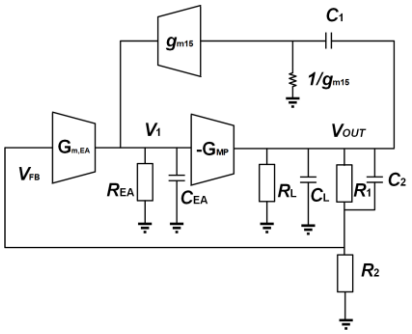


Figure 3. Small-Signal Model of the Complete Loop in the Proposed Scheme

In Figure 3, $G_{m,\,EA}$ represents the equivalent input transconductance of the error amplifier in the proposed scheme, G_{MP} denotes the transconductance of the power transistor, REA is the output resistance of the error amplifier, C_{EA} is the output capacitance of the error amplifier, RL stands for the LDO output resistance, gm15 indicates the transconductance of M_{15}, $1/g_{m15}$ corresponds to the equivalent input impedance of the common-gate amplifier formed by M_{15}, V_1 refers to the output voltage of the error amplifier, and VFB represents the feedback voltage.

This scheme incorporates an active feedback compensation technique by introducing an active capacitor C_1 between the drain of the PMOS power transistor and the source of the cascode device. This approach increases the frequency of the secondary pole while simultaneously employing a capacitor in parallel with the feedback resistor, collectively enhancing the stability of the loop.

3.2. Design of a Capacitor-Less LDO with Coupled-Structure Error Amplifier and Adaptive Biasing Circuit

To address the limitations of conventional capacitor-less LDOs, such as high power consumption, poor stability, and slow transient response, Xie Haiqing et al. developed a low-power, high-stability, and high-transient-response capacitor-less low-dropout regulator (LDO) based on Nuvoton 0.35μm CMOS technology [10].

The key innovation of this design lies in the use of a cross-coupled structure in the error amplifier. By adjusting the ratio of the coupled pairs, the architecture achieves a relatively large bandwidth and high gain under low quiescent current conditions, thereby significantly enhancing the overall system stability. Furthermore, the circuit incorporates an adaptive biasing structure that dynamically tracks load current variations. This mechanism supplies bias current to the preceding error amplifier according to operational demands, increasing the loop bandwidth and further improving the transient response of the LDO.

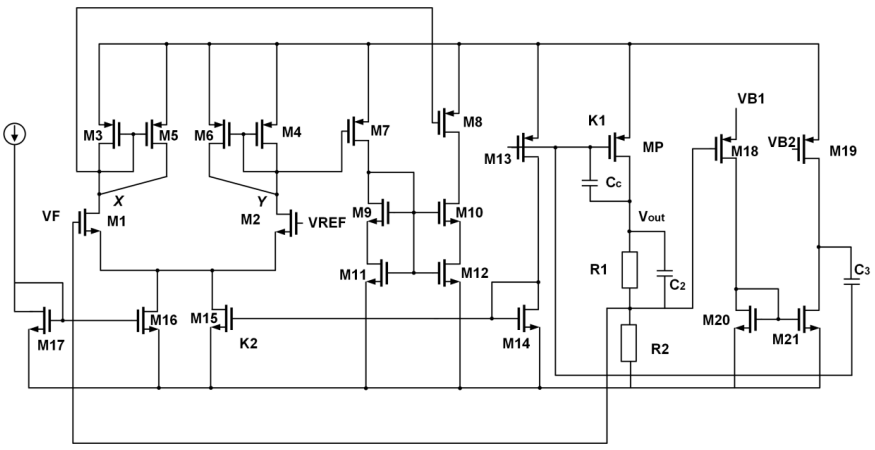


Figure 4. Circuit Schematic of the Proposed LDO Scheme

The LDO circuit designed in this scheme is illustrated in Figure 4. It consists of an error amplifier (EA), a power transistor, an adaptive bias circuit, feedback resistors, and a transient enhancement structure.

In this design, the error amplifier employs a two-stage topology: the first stage is a cross-coupled pair (composed of M1–M6), and the second stage is a self-biased cascode structure (composed of M7–M12). The bias current source for the EA includes both a fixed bias current It and an adaptive bias current IF that varies with the load current. The adaptive bias circuit is formed by M13–M15, wherein M13 and the large-sized power transistor MP constitute a high-ratio current mirror. The current through the power transistor IP is mirrored by M13 and further mirrored via M14 to M15. The feedback network is made up of resistors R1 and R2, while the compensation network includes a Miller capacitor C_C and a feedforward capacitor C_2. Additionally, a transient enhancement structure formed by M18–M21, in conjunction with a coupling capacitor C_3, is incorporated to improve transient performance.

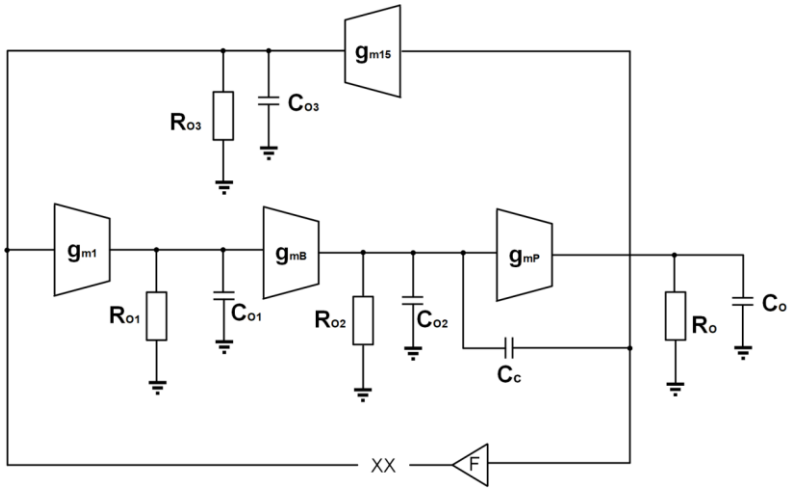


Figure 5. Equivalent Small-Signal Model of the Proposed LDO

The equivalent small-signal model of the LDO constructed in this work is illustrated in Figure 5. Here, g_{m1} and g_{m2} represent the equivalent transconductance of the first and second stages of the error amplifier, respectively, gmp denotes the equivalent transconductance of the power transistor, and Ron represents the equivalent impedance at each node.

4. Limitations and Drawbacks of Existing Design Schemes and Recommendations for Future Research

In the design of low-quiescent-current, high-transient-response LDOs without off-chip capacitors, reducing the size of the power transistor to improve transient response may lead to reduced drive capability or increased on-resistance, thereby degrading the dropout performance of the LDO. Furthermore, while transconductance enhancement techniques contribute to performance optimization, they rely on device matching and specific structures. In the presence of process variations (such as threshold voltage fluctuations), the consistency of loop gain and unity-gain bandwidth will be affected, thereby undermining mass-production reliability. On the other hand, active feedback and compensation capacitors require precise design of parameters such as g_{m15}, resulting in poor adaptability across different application scenarios. Moreover, the approach of simply connecting a small capacitor in parallel with the feedback resistors to improve light-load stability may still fail to fully guarantee stability under extremely light loads or large-range load transients due to limitations in compensation frequency range.

To address the above limitations, future research could focus on the following directions for in-depth study and improvement.

First, a configurable power transistor structure could be designed to balance the trade-off between transient response, drive capability, and dropout performance.

Second, a programmable or adaptive active compensation network could be adopted, combined with digital-assisted circuits or analog feedback mechanisms, to dynamically adjust compensation parameters according to load conditions, thereby enhancing stability across the entire load range [11].

Additionally, a dynamic transconductance adjustment circuit could be introduced to automatically adjust the transconductance of the error amplifier based on actual operating conditions such as load current and supply voltage, effectively improving the system's robustness against process fluctuations and its adaptability in diverse application scenarios.

In the off-chip-capacitor-free LDO architecture based on a cross-coupled error amplifier and an adaptive bias circuit, although the cross-coupled structure helps enhance gain and bandwidth, the noise introduced by the coupled pairs accumulates, potentially deteriorating the LDO's output noise performance and making it difficult to meet the stringent requirements of noise-sensitive applications. Furthermore, the transient enhancement structure has relatively high circuit complexity, which not only increases layout area but also makes its compensation effect highly dependent on process parameters, thereby raising mass-production costs and uncertainty. Meanwhile, the current mirror formed by M13–M15 is susceptible to issues such as threshold voltage mismatch and channel-length modulation effects, resulting in limited mirroring accuracy. This leads to insufficient matching between the adaptive bias current and the load current, thereby restricting the dynamic adjustment capability of the loop bandwidth.

To address these shortcomings, future research could focus on the following improvements.

Conduct in-depth noise analysis and suppression for the cross-coupled structure—for example, by employing "noise-canceling" techniques such as complementary coupling pairs or selecting low-noise devices—to effectively reduce output noise while maintaining high gain and bandwidth.

Enhance implementation efficiency through structural simplification, such as adopting a hybrid compensation scheme that combines "passive compensation with lightweight active assistance" to reduce circuit complexity and area overhead without compromising transient performance.

Additionally, consider implementing this architecture in more advanced process nodes, leveraging the high intrinsic speed of smaller devices to further extend loop bandwidth and transient response speed.

5. Conclusion

This paper focuses on an in-depth study of LDO chips without off-chip load capacitors. It begins by elucidating the critical role of LDO chips in the field of power management and reviews current research hotspots, followed by an explanation of the fundamental theory of LDO circuits. Regarding the research focus on off-chip capacitor-free designs, the limitations of traditional solutions are identified. Subsequently, two mainstream improved schemes for off-chip capacitor-free LDOs are comprehensively discussed: one emphasizing low quiescent current and high transient response, and the other based on a cross-coupled error amplifier and adaptive biasing circuitry. The existing shortcomings and constraints of these two approaches are also addressed, along with targeted proposals for future optimization directions such as configurable power transistors, noise cancellation, and structural simplification. These insights provide valuable reference for designing better low-power, fast-transient-response, off-chip capacitor-free LDO solutions in the future.

References

[1] Wang Y, He L T. CMOS Linear Regulators. Beijing: Science Press, 2012.

[2] Zhang Z W. Design of an Extremely Low-Power Capacitorless LDO Chip. Wuhan: China University of Geosciences, 2023.

[3] Kim Y I, Lee S S. A Capacitorless LDO Regulator With Fast Feedback Technique and Low-Quiescent Current Error Amplifier. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60 (6): 326–330.

[4] He T. Research and Design of a Capless LDO for MCU Applications. Xiamen: Xiamen University of Technology, 2023.

[5] Kong P. Research and Design of a Capacitorless LDO with Fast Transient Response and High Power Supply Rejection. Wuhan: Huazhong University of Science and Technology, 2022.

[6] Yao R H, Wang C, Kuang G H. Research and Development of Capacitorless LDOs. China Integrated Circuit, 2018, 27 (03): 30–38.

[7] Zhang M W. Power Supply Design of Low-Dropout Linear Regulator for Analog-to-Digital Converters. Nanjing: Southeast University, 2023.

[8] Ming X, et al. A Fast-Transient Capacitorless LDO With Dual Paths Active-Frequency Compensation Scheme. IEEE Transactions on Power Electronics, 2022, 37 (9): 10332–10347.

[9] Tian L, Yin Y S, Deng H H. Design of a Low-Quiescent-Current High-Transient-Response Capacitorless LDO. Microelectronics, 2024, 54 (02): 214–220.

[10] Xie H Q, Cao W, Cui K Y, et al. Design of a Low-Power High-Stability LDO. Electronic Design Engineering, 2024, 32 (14): 115–120.

[11] Yu H. A Capacitorless LDO with Programmable Soft-Start and Fast Load Transient Response. Wuhan: Wuhan University of Science and Technology, 2024.