Academic Journal of Science and Technology
ISSN: 2771-3032 | Vol. 23, No. 2, 2026

A Low-Drift, High-PSRR Bandgap Reference Using Piecewise Exponential Compensation and Internal Supply Regulation

Yicheng Cheng[1, *]

[1]Harbin University of Science and Technology, Harbin, China
[*]Corresponding author: 2504070103@stu.hrbust.edu.cn

Abstract: A bandgap reference based on high order temperature compensation and an integrated negative feedback voltage regulation technique has been designed. The proposed bandgap reference exhibits low temperature drift and high power supply rejection ratio (PSRR). By employing two pairs of MOS transistors operating in the subthreshold region, exponential compensation currents are generated in segmented fashion according to the operating temperature, thereby achieving high order temperature compensation and reducing the bandgap reference's temperature coefficient. Furthermore, leveraging the bandgap reference's output voltage, an integrated negative feedback regulation circuit is employed to enhance its PSRR. Using 0.18μm BCD process, the design, layout, and post-simulation verification of a low temperature-drift, high PSRR bandgap reference were completed. The layout area of the bandgap reference is 290μm×200μm. Post simulation results indicate that, over the temperature range of −45°C to 125°C, the temperature coefficient is only 1.15 × 10^{-6}/°C, and the PSRR reaches 83.22dB. Under a supply voltage variation from 2.8V to 5.5V, the average reference voltage is 1.212V, with a line regulation of 0.015%.

Keywords: Bandgap reference; higher order temperature compensation; temperature coefficient; power supply rejection ratio.

1. Introduction

The bandgap reference is an indispensable and critical module in integrated circuit design. It generates a reference voltage that is virtually immune to variations in temperature, supply voltage, and process parameters, making it widely used in analog and mixed signal systems. High precision data converters, sensor chips, battery-monitoring chips, and other applications demand bandgap references with lower temperature coefficients and higher PSRR to meet system-level requirements.

Because the VBE voltage of bipolar transistors exhibits a high order nonlinear temperature coefficient, conventional first order temperature compensation struggles to achieve a bandgap reference with a low temperature coefficient[1]. In recent years, many researchers have proposed bandgap reference architectures with excellent performance. For instance, Y. Liu et al. introduced a switched capacitor bandgap reference with second order curvature compensation for ultra low power systems; however, its temperature coefficient is 1.76 × 10^{-6}/°C. X. Ming et al. employed a piecewise exponential technique to realize a BiCMOS bandgap reference featuring higher order curvature compensation, achieving a favorable temperature coefficient, though its PSRR performance degrades at high frequencies. O. E. Mattia et al. implemented an ultra low power bandgap reference by leveraging a novel resistorless bipolar transistor biasing and curvature compensation circuit. B. Ma et al. proposed a novel CMOS bandgap reference that utilizes MOS transistors operating in the subthreshold region to achieve higher order curvature compensation.

This paper presents a high order temperature compensation circuit that employs two pairs of MOS transistors operating in the subthreshold region to generate an exponential type compensation current, which is then passed through resistors to achieve high order temperature compensation, thereby reducing the temperature coefficient of the bandgap reference. In addition, an integrated negative feedback voltage regulation circuit is designed to supply power to the core circuitry of the bandgap reference, effectively enhancing the overall circuit's power supply rejection performance.

2. Traditional First-Order Compensated Bandgap Reference

Traditional bandgap references exploit the positive temperature coefficient of the base emitter voltage difference ΔVBE between two bipolar transistors to compensate for the negative temperature coefficient of the base emitter voltage VBE. By summing these two terms with a specific weighting factor, a reference voltage VREF with zero temperature coefficient is obtained[2][3].

Figure 1 shows the circuit structure of a conventional first order compensated bandgap reference. In this circuit, transistor Q2 has an area n times that of Q1, and transistors M3, M4, and M5 have identical dimensions; resistor R2 equals R3. Due to the opamp feedback, voltages X and Y are equal, so the current IC1 equals IC2. From the relationship |VBE1| = |VBE2| + IC2R1, we obtain IC2 = VT ln(n) / R1. IC2 is mirrored through R2 to produce current IR4, whose expression is:

$$I_{R4} = \frac{V_T \ln n}{R_1} + \frac{|V_{BE1}|}{R_2}$$

Therefore, the magnitude of the bandgap reference output voltage VREF is:

$$V_{BEF} = \frac{R_4}{R_2} | V_{BE1} | + \frac{R_4}{R_1} V_T \ln n$$

By adjusting the values of resistors R1 and R2, VREF can be made to have a zero temperature coefficient. However, VBE is not perfectly linear; its temperature characteristics are:

$$V_{BE}(T) = V_G + [V_{BE}(T_0) - V_G(T_0)] \times \frac{T}{T_0} - (4 - n - \alpha)V_T \ln \frac{T}{T_0}$$

As shown by the above equation, VBE exhibits high order nonlinearity, whereas conventional bandgap references can only compensate the linear term corresponding to the second term in the expression. This limitation constrains the temperature coefficient of the bandgap reference[4][5][6]. To achieve a bandgap reference with lower temperature drift over a wider temperature range, it is necessary to implement higher order compensation for the exponential term in the third term of the VBE voltage expression.

Furthermore, the bandgap reference shown in Figure 1 is highly sensitive to the supply voltage, with a power supply rejection ratio that typically does not exceed 60dB, which is insufficient for high precision system applications[7].

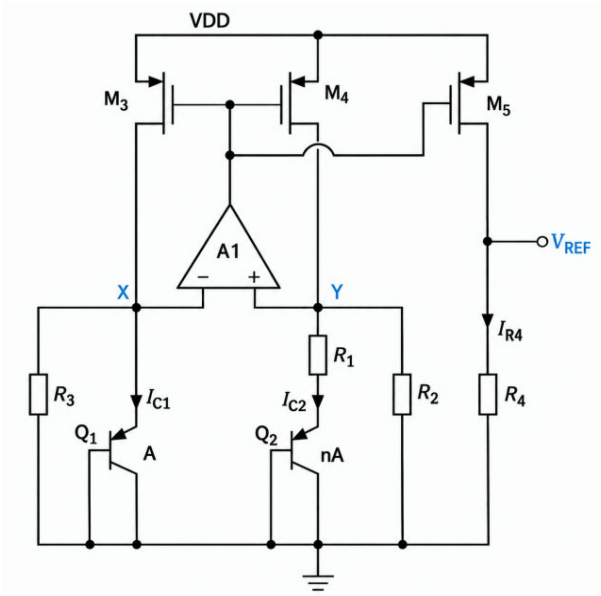


Figure 1. Circuit structure of a conventional first order compensated bandgap reference.

3. Low-Temperature-Drift, High PSRR Bandgap Reference Circuit Design

3.1. Reference Core Circuit

The core circuit of the bandgap reference designed in this paper is shown in Figure 2. It consists of a reference generation circuit and a higher order temperature compensation circuit. The reference generation circuit produces both a positive temperature-coefficient voltage and a negative temperature coefficient voltage, which are combined to generate a zero-temperature-coefficient output voltage V_{REF}. The higher order temperature compensation circuit comprises two pairs of MOS transistors operating in the subthreshold region; depending on the operating temperature, it generates an exponential compensation current $I_{comp.}$ This current flows through the compensation resistor R_{10}, producing a higher order temperature compensation voltage that adjusts the temperature coefficient of V_{REF}.

In Figure 2, the area of Q_7 is m times that of Q_6, and $R_6 = R_7$. Due to the opamp's clamping effect, the voltages at nodes V_3 and V_2 are equal, so $I_2 = I_3$. The difference ΔV_{BE} between the base emitter voltages of Q_6 and Q_7 can be expressed as:

$$\Delta V_{BE} = V_T \cdot \ln m = \frac{kT}{q} \cdot \ln m$$

Therefore, the current I_3 flowing through R_8 is:

$$I_3 = \frac{\Delta V_{BE}}{R_8} = \frac{kT}{q}\frac{\ln m}{R_8}$$

The current I_5 is the sum of I_2 and I_3; it flows through R_9 and R_{10}, generating a voltage V_5 with a positive temperature coefficient, whose expression is:

$$V_5 = (I_2 + I_3) \cdot (R_9 + R_{10}) = 2\frac{kT}{q}\frac{R_9 + R_{10}}{R_8} \ln m$$

The voltage V_{REF} is the sum of the base emitter voltage V_{BE6} of Q_6 and the voltage V_5, expressed as:

$$V_{REF} = V_{BE6} + 2\frac{kT}{q}\frac{R_9 + R_{10}}{R_8} \ln m$$

V_{BE6} has a negative temperature coefficient, while V_5 has a positive temperature coefficient; by adjusting the ratio of the resistors, V_{REF} can be made to have a zero temperature coefficient.

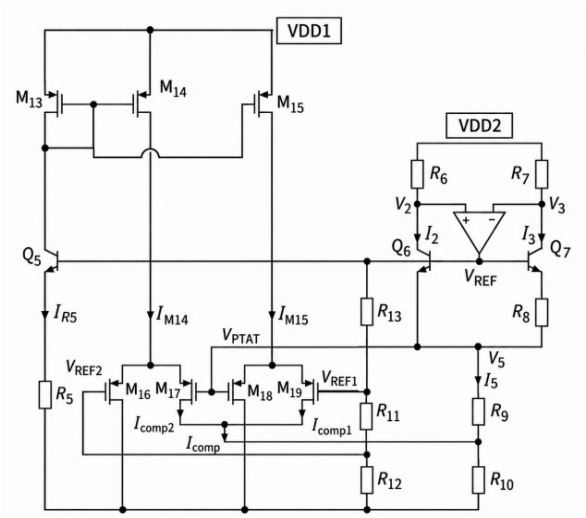


Figure 2. Core circuit of the bandgap reference.

3.2. Higher-Order Temperature Compensation Circuit

As shown in Figure 2, an exponential type compensation current can be generated by employing a differential pair operating in the subthreshold region. Figure 3 illustrates the principle behind the generation of this exponential current: the differential pair receives input voltages V_{REFX} (in Figure 2, V_{REFX} is obtained by voltage division across R_{11}, R_{12}, and R_{13} connected in series) and a voltage V_{PTAT} that varies linearly with absolute temperature (in Figure 2, this is V_5). The differential pair produces a temperature compensating current I_{comp}, which flows through resistor R_{10} to generate a compensation voltage, thereby compensating the reference voltage. Here, the currents I_{M14} and I_{M15} are on the order of 1μA, and the width-to-length ratios of M_{16}–M_{19} are designed to be as large as possible to ensure operation in the subthreshold regime. The following section analyzes the underlying mechanism for generating the exponential

compensation current.

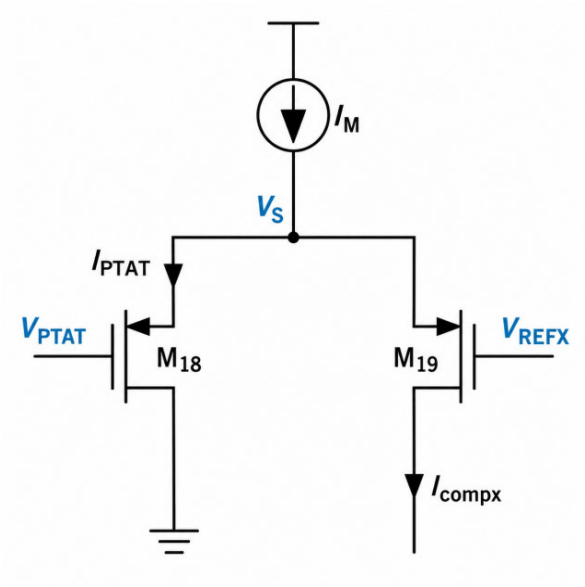


Figure 3. Circuit for generating exponential compensation current.

For a PMOS transistor, assuming that the voltage $V_{REFX} \gg V_{PTAT}$, then $I_{PTAT} \approx I_M$. The subthreshold current expression for a MOS transistor is known to be:

$$I_D = I_0 e^{\frac{|V_{GS}|-|V_{TH}|}{\eta V_T}}$$

According to Equation (9), the expression for V_s is:

$$V_s = \eta V_T \cdot \ln\frac{I_M}{I_o} + V_{PTAT} + |V_{THP}|$$

Then the compensation current I_{compx} can be expressed as:

$$I_{cmopx} = I_0 \cdot e^{\frac{V_S - V_{REFX} - V_{THP}}{\eta V_T}} = I_M \cdot e^{\frac{V_{PTAT} - V_{REFX}}{\eta V_T}}$$

The relationship between the positive-temperature-coefficient voltage V_{PTAT} and V_{REFX} can be expressed as $V_{PTAT} = aPTAT(T - T0) + V_{REFX}$, where aPTAT is the temperature coefficient of V_{PTAT} and T_0 is the temperature at which V_{PTAT} and V_{REF} intersect. Consequently, the compensation current I_{compx} can be simplified to:

$$I_{cmopx} = I_M \cdot e^{\frac{a_{PTAT}\cdot\Delta T}{\eta V_T}} = I_M \cdot e^{\frac{a_{PTAT}}{\eta k/q}\cdot\frac{\Delta T}{T_0+\Delta T}} = I_M \cdot e^{k_1\Delta T}$$

$$k_1 = \frac{a_{PTAT}}{\eta(k/q)(T_0 + \Delta T)}$$

In the equation, $\Delta T = T - T_0$. Consequently, within a relatively small range of ΔT ($\Delta T \ll T_0$), the compensation current increases exponentially as ΔT grows.

When the voltage $V_{REFX} \ll V_{PTAT}$, the input voltages at the two ends of the differential pair in Figure 3 are swapped. At this point, the compensation current I_{compx} can be expressed as:

$$I_{cmopx} = I_M \cdot e^{\frac{V_{REFX} - V_{PTAT}}{\eta V_T}}$$

In the temperature compensation circuit shown in Figure 2, the compensation circuit employs two differential pairs to generate two compensation currents; the total compensation current is expressed as $I_{comp} = I_{comp1} + I_{comp2}$. As indicated in Figure 2, the relationship between V_{PTAT} and the two voltage-divider voltages V_{REF1} and V_{REF2} is as follows: $V_{REF1} \gg V_{PTAT}$, and $V_{REF2} \ll V_{PTAT}$. Consequently, based on Equations (11) and (14), the expressions for the compensation currents I_{comp1} and I_{comp2} are:

$$I_{compl} = I_{M14} e^{\frac{V_{PTAT} - V_{REFl}}{\eta V_T}}$$

$$I_{comp2} = I_{M15} e^{\frac{V_{REF2} - V_{PTAT}}{\eta V_T}}$$

Among them:

$$V_{REF1} = \frac{R_{11} + R_{12}}{R_{11} + R_{12} + R_{13}} \cdot V_{REF}$$

$$V_{REF2} = \frac{R_{12}}{R_{11} + R_{12} + R_{13}} \cdot V_{REF}$$

As shown by Equations (15)–(18), $V_{REF1} > V_{REF2}$, and the waveform of the compensation current is illustrated in Figure 4. The compensation current flows through resistors, generating two compensation voltages that respectively compensate for the low temperature and high temperatur e regions of the bandgap reference. By trimming the values of the series voltage divider resistors R_{11} and R_{12} in Figure 2, the magnitude of the compensation current can be adjusted, thereby controlling the magnitude of the compensation voltages and raising the curve of the bandgap reference voltage in both the low temperature and high temperature ranges to near the level observed at the mid temperature point. In this way, by applying two exponential high order compensation voltages to the exponential term in the third term of Equation (3) for the V_{BE} voltage, a higher order compensation is achieved for V_{REF}. The compensated bandgap reference voltage can then be expressed as:

$$V_{REF,COMP} = V_{REF} + (I_{comp1} + I_{comp2}) \cdot R_{10}$$

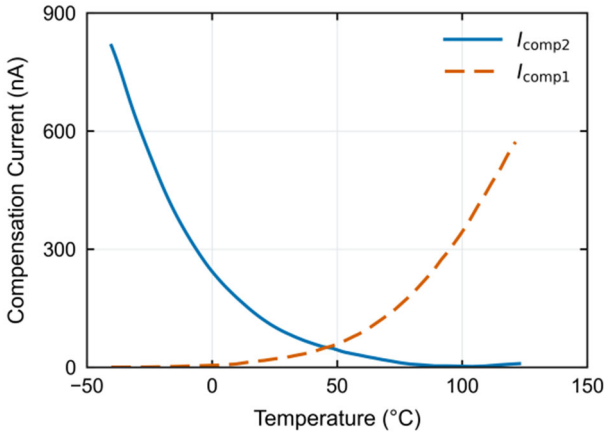


Figure 4. Waveform of the compensation current.

Therefore, by adding two compensation voltages to the uncompensated bandgap reference voltage V_{REF}, we obtain the final bandgap reference voltage $V_{REF,COMP}$, thereby improving the temperature coefficient of the bandgap reference. The schematic curves before and after bandgap compensation are shown in Figure 5: the uncompensated bandgap reference exhibits a sawtooth like curve, whereas after compensation, both ends of the curve—corresponding to

the low temperature and high temperature regions—are lifted, resulting in a wavy shaped curve. In general, a conventional first order compensated bandgap reference can achieve a temperature coefficient of approximately 1.5×10^{-5}/°C, while a higher order compensated bandgap reference can attain a temperature coefficient of 2×10^{-6}/°C or lower.

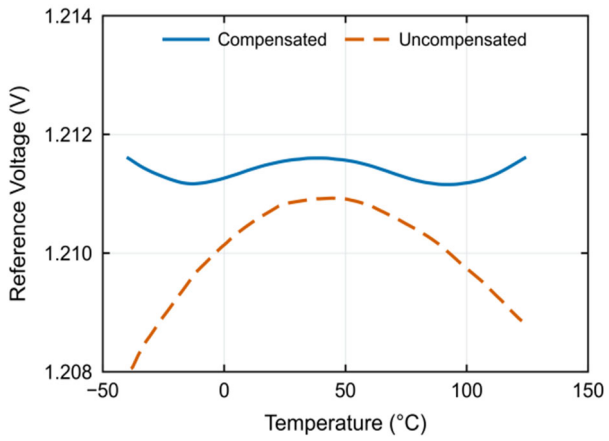


Figure 5. Schematic curves of the bandgap reference before and after compensation.

3.3. Bandgap Reference Overall Circuit

Figure 6 shows the overall circuit of the designed bandgap reference, which comprises a startup circuit, a voltage regulation circuit, a biasing circuit, a temperature compensation circuit, and a reference generation circuit. In the figure, VDD1 is the supply voltage that powers all circuits except the reference generation circuit; VDD2 is the output voltage of the internal negative feedback voltage regulation circuit and supplies power to the reference generation circuit.

When the circuit is powered on and starts up, R_2, Q_2, and Q_0 turn on. At this point, the voltage at node V_1 equals the sum of the V_{BE} of transistors Q_0 and Q_2, which is approximately 1.4 V. Consequently, during startup, Q_3 turns on first, followed by the sequential turn on of Q_5, Q_6, and Q_7, allowing current to flow. Subsequently, under the feedback action of the amplifier, the bandgap reference raises V_{REF} to around the bandgap reference voltage of 1.2V. At this stage, Q_3 turns off, completing the startup process.

In Figure 6, the reference generation circuit is powered by VDD2. When the supply voltage VDD1 varies or fluctuates, the magnitude of VDD2 remains nearly constant, thereby ensuring that V_{REF} is unaffected by variations in the supply voltage and effectively improving the power supply rejection ratio. The operating principle of the voltage regulation circuit is as follows: when the supply voltage fluctuates or for other reasons causes VDD2 to change, the base voltage of Q_1 also adjusts accordingly, maintaining a constant current through R_1 (the current through M_8 is an exact replica of I_{R5}, with $I_{D8} = I_{R5} = (V_{REF} - V_{BE5}) / R_5$). At this point, the negative feedback loop formed by Q_1, M_5, M_3, M_4, M_6, R_1, and M_8 suppresses changes in VDD2, keeping it stable. Notably, M_6 must be sized sufficiently large to provide ample current to the bandgap reference core circuit. Capacitor C serves as a compensation capacitor, ensuring adequate phase margin in the regulation loop and preventing oscillation. VDD2 can be expressed as:

$$\begin{aligned} VDD2 &= V_{REF} + V_{BE1} + I_{DB} \cdot R_1 \\ &= V_{REF} + V_{BE1} + (V_{REF} - V_{BE5}) \cdot \frac{R_1}{R_5} \end{aligned}$$

Through derivation and subsequent simulation verification, it can be determined that the value of VDD2 is approximately 2.5V. As shown in Equation (20), VDD2 depends solely on the resistor ratio and process parameters, and is independent of the supply voltage VDD1. Consequently, when the supply voltage varies, VDD2 remains constant, thereby enhancing the power-supply rejection ratio and line regulation of the bandgap reference.

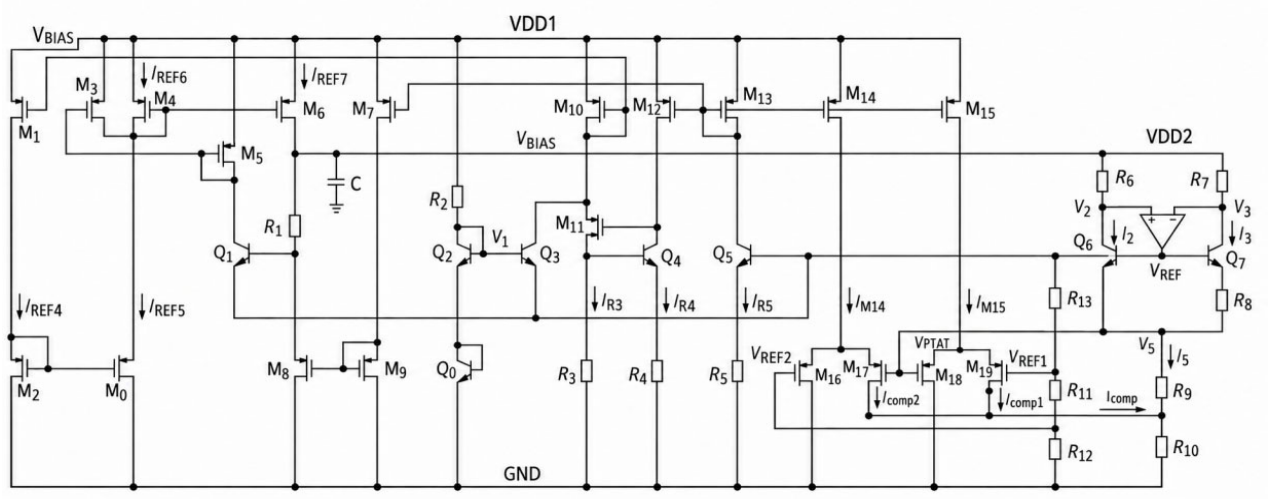


Figure 6. Overall circuit of the bandgap reference.

4. Post-Simulation Results

This design is based on the Dongbu 0.18μm BCD process; the layout of the bandgap reference is shown in Figure 7, with an area of 290μm × 200μm. The designed bandgap reference has a typical operating voltage of 5V, and the post simulation results are as follows.

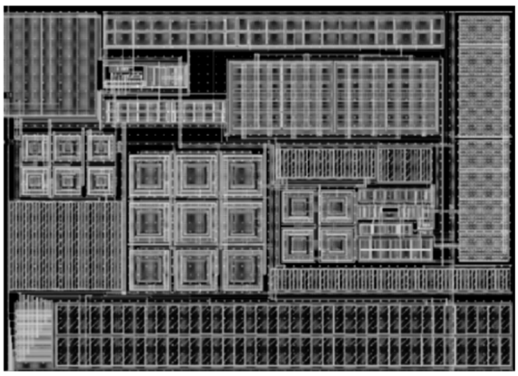


Figure 7. Layout of the designed bandgap reference.

Figure 8 shows the temperature dependent output characteristic curve of the bandgap reference without high order compensation.

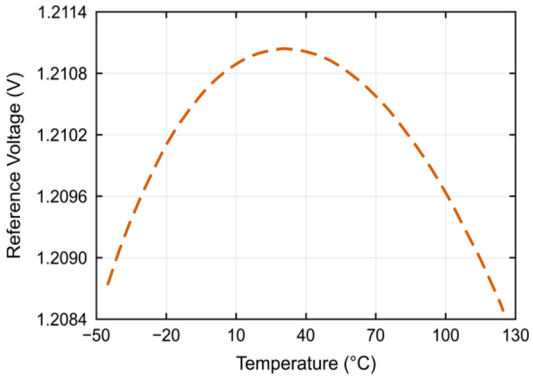


Figure 8. Temperature characteristic curve of the uncompensated bandgap reference.

Simulation results show that, under the TT process corner and within a temperature range of −45 to 125°C, the uncompensated output reference voltage has an average value of 1.210V and a temperature coefficient of 1.241 × 10^{-5}/°C. In contrast, after applying the proposed high order temperature compensation, the bandgap reference's output temperature characteristic curve shown in Figure 9 exhibits an average output voltage of 1.2122V and a temperature coefficient of 1.15 × 10^{-6}/°C. As illustrated in Figure 9, the compensated temperature characteristic curve transitions from a flat top shape to a wavy profile, with a significant reduction in the temperature coefficient. Figure 10 presents a comparison of the temperature characteristics before and after compensation.

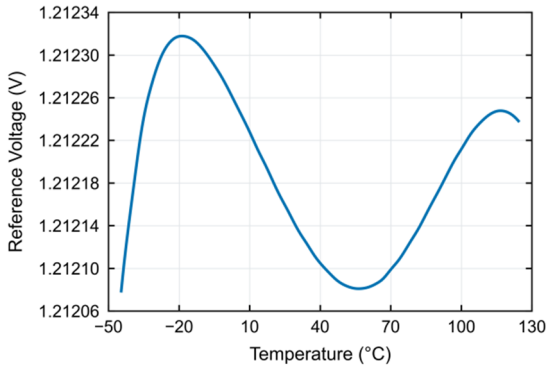


Figure 9. Temperature characteristic curve of the compensated bandgap reference.

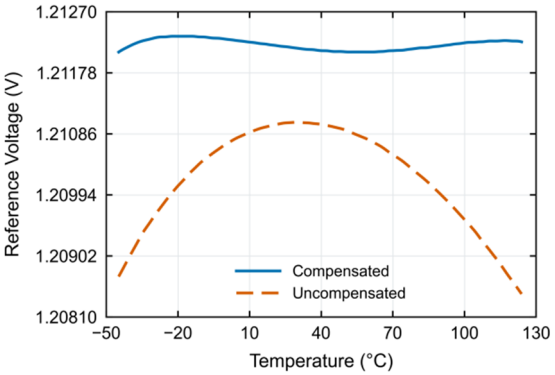


Figure 10. Comparison of temperature characteristics before and after compensation.

Figure 11 shows the post layout simulation results of the designed bandgap reference under different process corners. Under various process corners, the adjusted output voltage varies from 1.191V to 1.228V, while the temperature coefficient ranges from 1.15 × 10^{-6}/°C to 6.01 × 10^{-6}/°C.

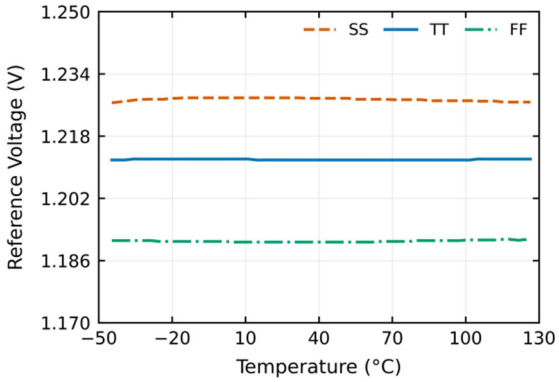
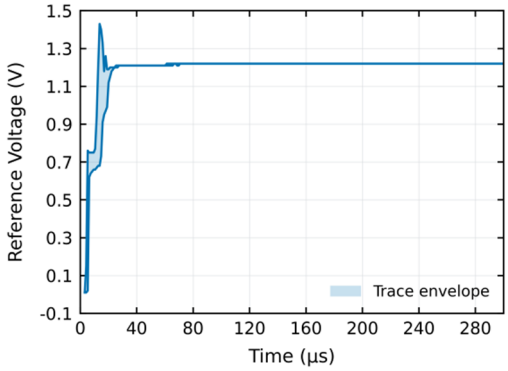
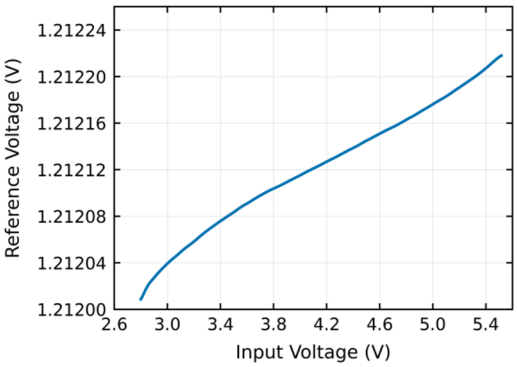


Figure 11. Temperature characteristic curves of the output reference voltage under different process corners.

Figure 12(a) . shows the transient output waveform of the designed bandgap reference over a supply voltage range of 2.8 to 5.5V. The simulation results indicate that the designed bandgap reference can reliably start up and deliver the reference voltage across this voltage range. Figure 12(b). presents the simulation results for the line regulation of the designed bandgap reference, which is 0.015%.



(a) Output waveform



(b) Line regulation

Figure 12. Output waveform and line regulation of the bandgap reference under different supply voltages.

Figure 13 shows the power supply rejection ratio (PSRR) characteristic curve of the bandgap reference designed in this paper. Thanks to the integrated negative feedback voltage regulation circuit that supplies power to the reference's core circuitry, the PSRR of the proposed bandgap reference reaches 83.22dB at low frequencies; moreover, over the 1–10kHz frequency range, the PSRR remains above 80dB.

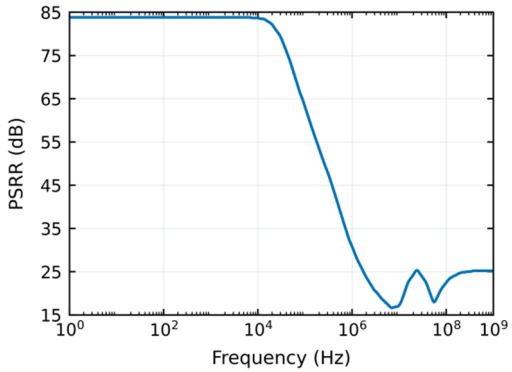


Figure 13. PSRR characteristic curve of the bandgap reference voltage.

Table 1 presents a summary of the parameters of the bandgap reference designed in this paper, along with a performance comparison to other references. As the comparison shows, the proposed bandgap exhibits a low temperature coefficient and a high power supply rejection ratio, making it suitable for high precision system applications.

5. Conclusion

This paper presents a bandgap reference with high PSRR and low temperature coefficient, designed based on the Dongbu 0.18μm BCD process. It employs segmented higher order temperature compensation and PSRR enhancing techniques. By utilizing MOS differential pairs operating in the subthreshold region and adopting a segmented higher order temperature compensation scheme, the bandgap reference achieves a low temperature coefficient. Additionally, an integrated negative feedback voltage regulation technique is employed to attain a high power supply rejection ratio. Post layout simulation results indicate that the proposed bandgap reference exhibits a PSRR of 83.22dB and a temperature coefficient of 1.15 × 10^{-6}/°C, demonstrating both high PSRR and low temperature drift, making it well suited for applications such as high precision analog-to-digital conversion circuits.

Table 1. Summary of Parameters of the Designed Bandgap Reference and Comparison with Relevant Literature

Parameter	[8]	[9]	[10]	[11]	This work
Process/μm	0.18	0.18	0.18	0.5	0.18
VDD/V	1.2	5	1.8	5	2.8~5.5
Reference /V	0.767	1.3	0.6	1.24	1.212
TC(×10-6/°C)	3.4	4.46	0.94	14.2	1.15
Temperature range/°C	-40~120	0~145	-40~125	-50~125	-45~125
PSRR/dB@10Hz	84	73.75	63.67	80	83.22
PSRR/dB@100Hz	84	73.75	63.67	62	83.22
PSRR/dB@1kHz	75	73.75	54.87	33	83.22
PSRR/dB@10kHz	55	73.20	36	7	83.09

References

[1] Jiang, H., & Mercier, P. P. (2018). A 0.4-V 0.93-nW/kHz relaxation oscillator exploiting comparator temperature-dependent delay to achieve 94-ppm/°C stability. IEEE Journal of Solid-State Circuits, 53(10), 3004–3011. https://doi.org/10.1109/JSSC.2018.2859834.

[2] Wang, L., & Zhan, C. (2019). A 0.7-V 28-nW CMOS subthreshold voltage and current reference in one simple circuit. IEEE Transactions on Circuits and Systems I: Regular Papers, 66(9), 3457–3466. https://doi.org/10.1109/TCSI.2019.2927240Amjady, N. (2001). Short-term hourly load forecasting using time-series modeling with peak load estimation capability. IEEE Transactions on Power Systems, 16(4), 798–805. https://doi.org/10.1109/TPWRS.2001.956757

[3] Huang, W., Liu, L., & Zhu, Z. (2021). A sub-200nW all-in-one bandgap voltage and current reference without amplifiers. IEEE Transactions on Circuits and Systems II: Express Briefs, 68(1), 121–125.

[4] Huang, Q., Zhan, C., Wang, L., Li, Z., & Pan, Q. (2020). A −40 °C to 120 °C, 169 ppm/°C nano-ampere CMOS current reference. IEEE Transactions on Circuits and Systems II: Express Briefs, 67(9), 1494–1498.

[5] Nagulapalli, R., Palani, R. K., & Bhagavatula, S. (2021). A 24.4 ppm/°C voltage mode bandgap reference with a 1.05V supply. IEEE Transactions on Circuits and Systems II: Express Briefs, 68(4), 1088–1092. https://doi.org/10.1109/TCSII.2020.3034256

[6] Osaki, Y., Hirose, T., Kuroki, N., & Numa, M. (2013). 1.2-V supply, 100-nW, 1.09-V bandgap and 0.7-V supply, 52.5-nW, 0.55-V subbandgap reference circuits for nanowatt CMOS LSIs. IEEE Journal of Solid-State Circuits, 48(6), 1530–1538. https://doi.org/10.1109/JSSC.2013.2252523

[7] Lin, J., Wang, L., Lu, Y., & Zhan, C. (2020). A nano-watt dual-output subthreshold CMOS voltage reference. IEEE Open Journal of Circuits and Systems, 1, 100–106. https://doi.org/10.1109/OJCS.2020.2995804

[8] Ma, Y., Bai, C., Wang, Y., & Qiao, D. (2020). A low noise CMOS bandgap voltage reference using chopper stabilization technique. In 2020 IEEE 5th International Conference on Integrated Circuits and Microsystems (ICICM) (pp. 184–187). IEEE.

[9] Dong, X., et al. (2025). A high power supply rejection and low temperature coefficient bandgap voltage reference. In 2025 7th International Conference on Circuits and Systems (ICCS) (pp. 45–49). IEEE.

[10] Wang, Q., Ma, T., & Wei, Q. (2025). A 2.2ppm, low-noise bandgap reference voltage circuit with stacked base-emitter voltage difference in 180nm BCD process. In 2025 7th International Conference on Circuits and Systems (ICCS) (pp. 6–11). IEEE.

[11] Lourenco, N., et al. (2022). Radiation-hardened bandgap voltage and current reference for space applications with 2.38 ppm/°C temperature coefficient. In 2022 18th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD) (pp. 1–4). IEEE.