

Design and Implementation of Precision Phase Measurement Module Base on Digital Dual Mixer Time Difference

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Abstract: Precise phase difference measurement is critical for distributed time synchronization systems. Aiming at the problem of how to realize the sub-nanosecond phase difference measurement of the time signal, the digital dual mixer time difference (DDMTD) measurement technology is used to measure the fine transmission delay and the two digital clock phase difference. Given the problem that it is difficult to generate a common clock source with fine frequency changes inside the FPGA chip, the Si5338 chip is used to generate 4 differential clocks, and the communication with the FPGA is completed through the I²C protocol, and the differential signal is converted into a single-ended clock source inside the FPGA as two. The common standard frequency of clock signals with the same frequency and different phases, realize the amplification of the phase difference measurement range, making the measurement accuracy reach sub-nanosecond level.

Keywords: Distributed time synchronization systems, Phase difference measurement, DDMTD.

1. Introduction

Both distributed real-time simulation systems and distributed coherent radars require high-precision time synchronization. Due to the extremely wide coverage of these facilities, the applicability of traditional point-to-point time synchronization methods is limited, and this distributed facility also poses a challenge to the synchronization accuracy that traditional time allocation systems can achieve[1]. In 2008, the European Organization for Nuclear Research (CERN) proposed the White Rabbit (WR) technology, which was designed to achieve sub-nanosecond distributed clock synchronization and data transmission with deterministic delay, for application in accelerator synchronization control. WR clock synchronization technology is an extension of IEEE 1588-2008 (PTP), mainly aimed at improving the accuracy of PTP clock synchronization and increasing time synchronization accuracy by one order of magnitude to meet the needs of large-scale scientific infrastructure for time synchronization. This technology combines multiple mature technologies such as Synchronous Ethernet (Sync-E), Precision Time Protocol (PTP), and digital dual mixing, and is a technology that utilizes fiber optics to achieve high-precision time-frequency transmission. By using the WR-PTP protocol and digital dual mixing phase detector to enhance timestamp accuracy, the synchronization accuracy can reach sub-nanosecond level due to the ability to accurately calculate and compensate for line delay asymmetry. Due to its fully open source, strong universality, and high accuracy, WR technology has received increasing technical support from research institutions and commercial companies[2]. Based on the White Rabbit protocol, the designers proposed an

improved scheme for digital dual mixer time difference (DDMTD) amplification technology to automatically adjust propagation delay and maintain phase alignment, resulting in clock jitter and clock deviation less than 100 ps[3].

DDMTD is a digital system that theoretically can use a relatively low-frequency counter to measure the time difference between two digital clock signals at very low resolution. The system is essentially a digital phase detector with femtosecond time resolution. The main issue with this processing technology is its feasibility and accuracy when implemented on FPGA. Another issue is the horizontal phase noise caused by the environment in digital signals. This noise will endanger the fidelity of the clock and cause faults in the signal. This article mainly verifies the feasibility of implementing DDMTD on FPGA and achieves sub-nanosecond measurement accuracy[4].

2. Principle of Digital Dual Mixer Time Difference (DDMTD)

The digital dual mixer time difference (DDMTD) measurement technology is a development of the analog dual mixer time difference measurement (DMTD) technology. DMTD is very useful for characterizing the clock stability of two clock signals (clk_1 and clk_2) with the same nominal frequency. By using a common offset clock, DMTD performs analog mixing and down-converts the two input clocks to low frequencies. After low-pass filtering, the resulting signal can be used to estimate the phase difference between the two clock signals.

2.1. Analog Dual Mixing time Difference

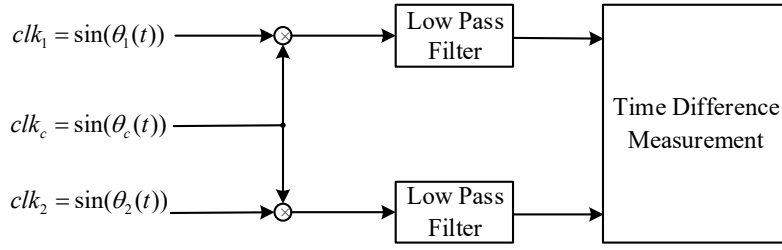


Figure 1. DMTD schematic diagram

Figure 1 shows the working principle of DMTD. Assuming the two input clock signals clk_1 and clk_2 have the following phase function:

$$\theta_1(t) = 2\pi\nu_0 t \quad (1)$$

$$\theta_2(t) = 2\pi\nu_0 t - \theta_{offset} \quad (2)$$

Where ν_0 is the frequency of the input clock, θ_{offset} is the phase shift of clk_2 relative to clk_1 , and the time difference between the two clocks is shown in the following equation:

$$\Delta t = \frac{\theta_{offset}}{2\pi\nu_0} \quad (3)$$

The phase function of the common clock source clk_c is as follows:

$$\theta_c(t) = 2\pi(\nu_0 - \nu_b)t \quad (4)$$

Where ν_b is the frequency difference, after passing the low-pass filter, the output clocks clk_1^{DMTD} and clk_2^{DMTD} have the following relationship:

$$\theta_1^{dmtd}(t) = \theta_1(t) - \theta_c(t) = 2\pi\nu_b t \quad (5)$$

$$\theta_2^{dmtd}(t) = \theta_2(t) - \theta_c(t) = 2\pi\nu_b t - \theta_{offset} \quad (6)$$

The two input clock signals defined in formulas (1) and (2) are converted into lower frequency clock signals while maintaining their phase shift θ_{offset} unchanged. A counter can be used to measure the time difference between clk_1^{DMTD} and clk_2^{DMTD} edges, represented by Δt^{DMTD} .

$$\Delta t^{DMTD} = \frac{\theta_{offset}}{2\pi\nu_b} \quad (7)$$

According to formulas (3) and (7):

$$\Delta t = \frac{\nu_b}{\nu_0} \Delta t^{DMTD} \quad (8)$$

2.2. Digital Dual Mixing time Difference

DDMTD uses digital mixing to generate an output clock signal with a frequency lower than the input clock signal. Figure 2 shows the working principle of DDMTD.

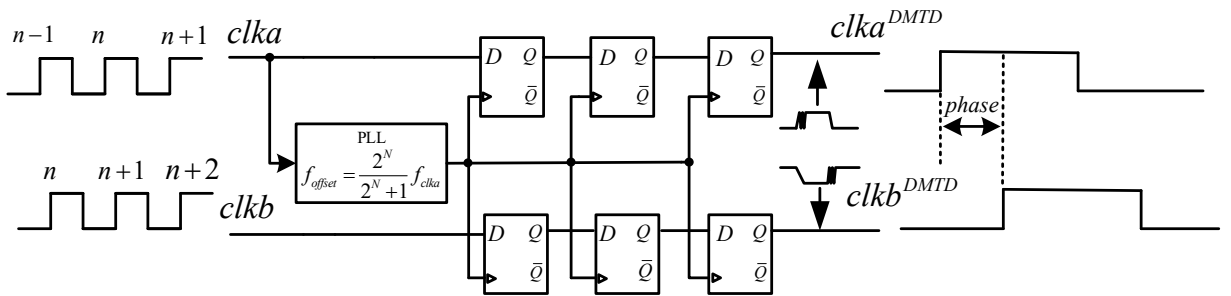


Figure 2. DDMTD phase detection principle diagram

The working principle of DDMTD is shown in Figure 2, $clka$ and $clkb$ represent the local clock and recovery clock in the data stream, respectively. They have the same frequency but different phases. The auxiliary clock signal is generated by an external phase-locked loop, and there is a slight difference between the frequency of the auxiliary signal and the measurement signal frequency $clka$, $clkb$. The frequency relationship between them satisfies the following equation:

$$f_{offset} = \frac{2^N}{2^N + 1} f_{clka} \quad (9)$$

After passing through a three-level D-flip-flop, the low-frequency clocks $clka^{DMTD}$ and $clkb^{DMTD}$ will be output. The sampling operation performed by the trigger is similar to analog mixing and low-pass filtering. The frequency of the output clock signals $clka^{DMTD}$ and $clkb^{DMTD}$ is significantly reduced, and the clock period available for measurement becomes larger.

The time difference between the edge of the output clock signal and the input clock signal is exactly $2^N + 1$ times linear relationship. The phase difference between input signals is equal to the phase difference between output signals. Therefore, by measuring the phase difference of the output

signal of the D-flip-flop, the phase difference of the measured signal can be obtained [4].

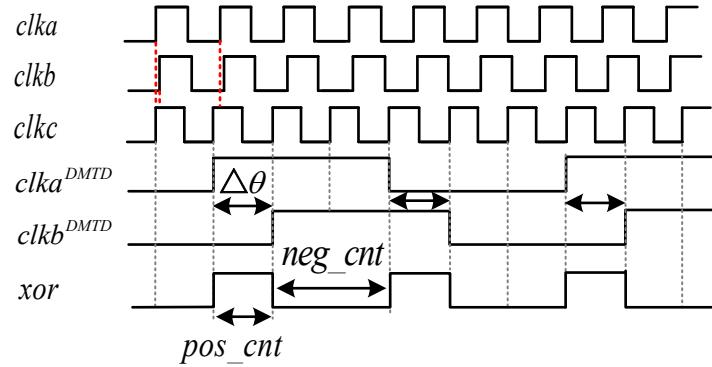


Figure 3. Schematic diagram of enlarged measurement range when N=1

Two clocks $clka$ and $clkb$ with the same frequency but different phase, triggered by an auxiliary clock $clkc$, just linearly amplify the measurement range of $clka$ and $clkb$ by $2^N + 1$ times. Figure 3 shows that when $N=1$, the output clock signal is amplified three times in the $clkc$ domain. As shown in Figure 3, xor is the XOR operation of clock signals $clka^{DMTD}$ and $clkb^{DMTD}$. When it is high level, it happens to be the phase difference between the two clocks. Count the high and low levels using a 500MHz clock, and within half a cycle of the output signal, the total phase is 180° . According to

formula (10), the phase difference between and can be calculated.

$$\Delta\theta = \frac{pos_cnt}{pos_cnt + neg_cnt} \times 180^\circ \quad (10)$$

Where pos_cnt is the count of the high-level of signal xor , neg_cnt is the count of the low-level of signal xor .

3. Module Design and Implementation

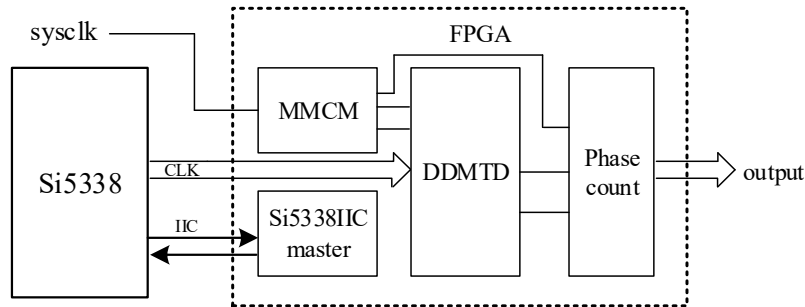


Figure 4. Digital Mixing Phase Discrimination Frame Diagram

The block diagram of the digital dual mixing phase discriminator is shown in Figure 4. Clocks of the same frequency but different phases are generated by the internal MMCM of the FPGA, and the common clock source is communicated with the Si5338 clock chip through the I²C protocol by the Si5338 control module. Storage files are configured to generate a common clock source for the Si5338 clock chip. The DDMTD module completes the mixing and low-pass filtering of two same-frequency clocks. The phase counting module counts the high and low levels of the two output signals after XOR, and measures the phase difference using equation (10).

3.1. Generation of Auxiliary Frequency

The key to DDMTD is the generation of auxiliary frequencies. Due to the frequency satisfying formula (9), there will inevitably be decimals, which is not easy to achieve with Verilog programming. The generation can be done in two ways:

(1) Calling the PLL or MMCM of FPGA to generate an auxiliary clock, the clock frequency and the frequency of the measured clock (clk_a and clk_b) satisfy the relationship of formula (9), and this scheme is only applicable to the case of

$1 \leq N \leq 5$. As the value of N increases, the frequency value of f_{offset} and f_{clka} become closer and closer. When $N > 5$, the auxiliary clock frequency generated by this method was equal to f_{clka} , and mixing effect could not be achieved at this time.

(2) Using clock chip Si5338 to generate auxiliary frequency. Si5338 is a high-performance, low jitter clock generator that can synthesize four user programmable clock frequencies. Si5338 adopts a two-stage synthesis architecture and high-resolution MultiSynth technology, which can generate four independent frequencies from one input frequency. In addition to generating a clock, the input can also bypass the synthesis stage, allowing Si5338 to be used as a high-performance clock buffer or as a combination of buffer and generator. For applications that require frequency tuning, such as clock margin tuning, each synthesized frequency can be incremented or decremented by a user-defined step, with a minimum step of 1 ppm. Output-to-output phase delays are also adjustable in user-defined steps with an error of <20 ps to compensate for PCB trace delays or for fine tuning of setup and hold margins. The zero delay mode also helps to minimize input to output delay.

The configuration and operation of Si5338 are controlled

by using the I²C interface to read and write RAM space. This device operates in a 7-bit addressing slave mode and can operate in standard mode (100 kbps) or fast mode (400 kbps), and supports burst data transmission with automatic address increment. The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL).

To simplify device configuration, Silicon Labs provides

ClockBuilder desktop software. This software has two purposes: to configure the optimal frequency division ratio for Si5338 based on the required frequency and to control the EVB. The optimal configuration can be saved in a text file from the software, which can be used in any system through I²C configuration.

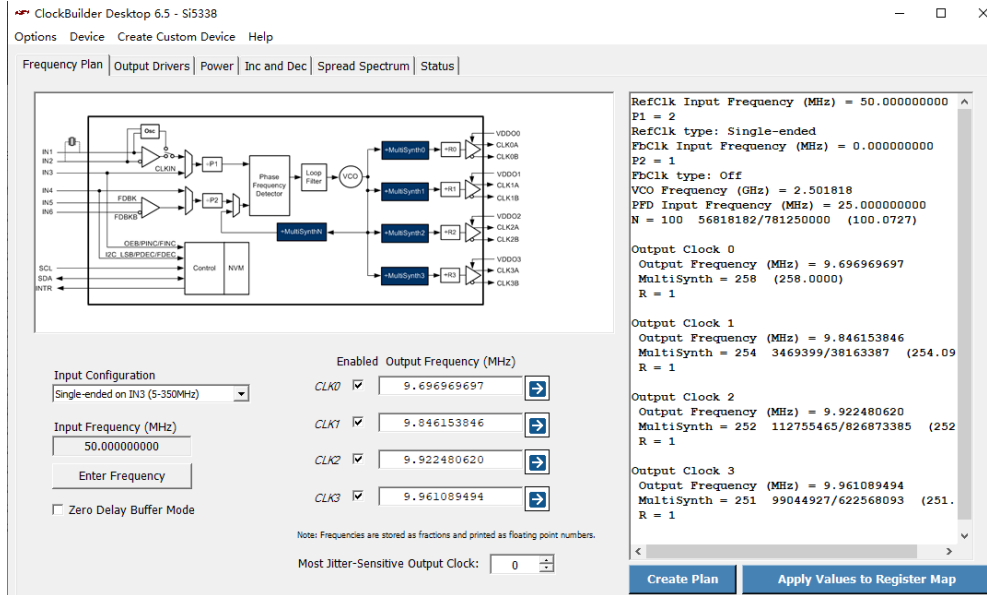


Figure 5. Si5338 Frequency Configuration Diagram

As shown in Figure 5, four output frequencies can be set each time, with an accuracy of up to 9 decimal places. When N is taken as 5, 6, 7, and 8, the auxiliary clock frequencies correspond to 9.6969697MHz, 9.846153846MHz, 9.922480620MHz, and 9.961089494MHz, respectively, when the measured clock is 10MHz. After setting all the parameters in Figure 6, save the C Code Header File, convert the C Header source file into a Si5338.mif file using a Python program, and add this file to the Memory Initialization Files folder in the Vivado project. If the N value is different, multiple mif files can be added at the same time. When instantiating the Si5338IIC master module at the top level of the project, modify the mif suffix file name to call the corresponding mif file, and complete the configuration of the Si5338 chip inside the FPGA.

3.2. Simulation and Test Results

Using modelism simulation, when N=5, the two output clock cycles are amplified 33 times, with a high level meter value of 103 and a low level meter value of 722. The phase difference is calculated according to equation (10), indicating that the function of measuring phase difference through digital dual mixing can be achieved.

The test verification is implemented through the XC7k325 board of ALINX. The input FPGA clock is 200MHz, and two same frequency clocks with a difference of 10° are generated through the MMCM of FPGA. When N takes different values, the generated bit stream file is burned into the development board, and multiple sum values of each N value are recorded in sequence, and the average value is calculated.



Figure 7. Upper board test diagram

Figure 7 shows the signals captured by Vivado's Integrated Logic Analyzer after the program is loaded. After burning the bitstream file into the development board, a trigger condition is required to display all desired waveforms. Here, the rising edge of Q3 is selected as the trigger condition. Due to the fact that the 4-way clock (differential to single-ended) generated by the FPGA external clock chip Si5338 has decimals, it

cannot be captured using ILA. Therefore, while performing digital dual mixing auxiliary frequency, we will control the four LED lights on and off of the Xc7k325 development board with the four clock signals. Four Led lights flashing at different frequencies indicate the successful configuration of the four clock frequencies.

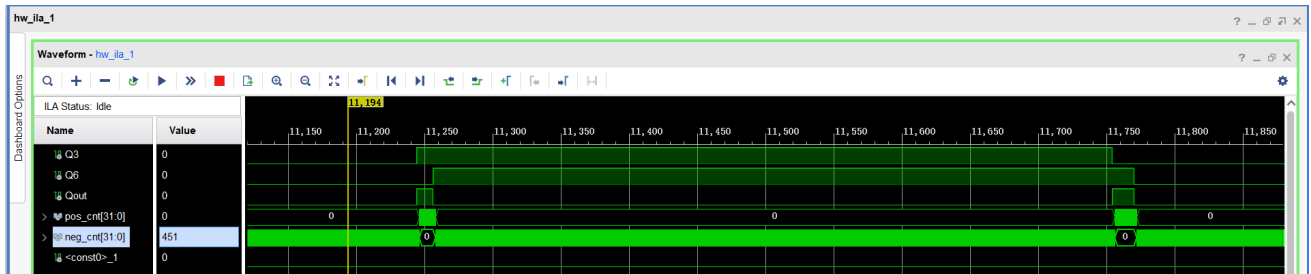


Figure 8. ILA Grasp Half Cycle Waveform Amplification

As shown in Figure 8, Q_{out} is the XOR of Q_3 (in Figure 2) and Q_6 (in Figure 2), $pos_cnt[31:0]$ and

$neg_cnt[31:0]$ are the counts of high and low levels respectively. The recorded data is averaged and recorded in Tables 1 and 2.

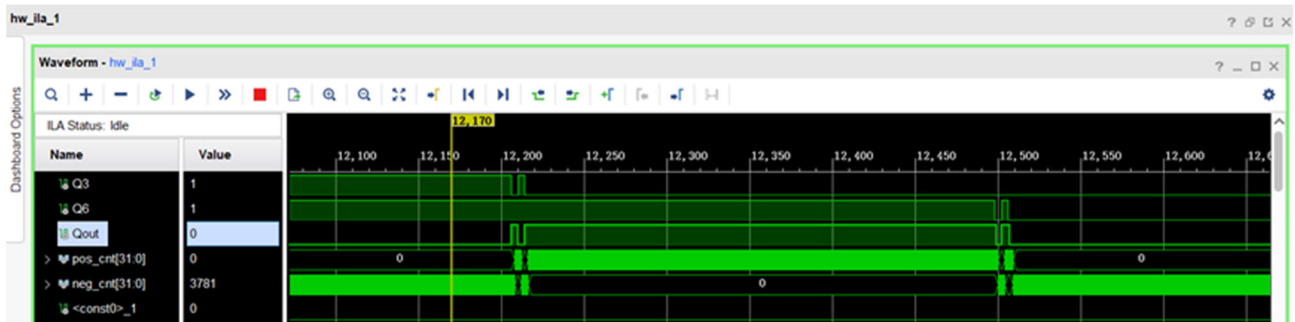


Figure 9. Jitter appear on the edge of the signal Qout when N increases to a certain value

As the N value increases, the probability of burrs appearing on the output clock edge also increases. As shown in Figure 9, when measuring the phase of two 10 MHz co frequency clocks, there will be burrs on the edge of the signal when N is

taken as 13. When measuring the phase of two 125 MHz co frequency clocks, when N is taken as 12, burrs will appear on the edges of the signal. At this point, due to high and low level jumps, the counting will be inaccurate.

Table 1. Phase Counting Measurement of 500MHz to 10MHz Signal

N	2^N	$2^N + 1$	f_{offset} (MHz)	pos_cnt	neg_cnt	$\Delta\theta$ ($^\circ$)
3	8	9	8.888888889	57	168	45.600
4	16	17	9.411764706	22	148	23.294
5	32	33	9.696969697	53	372	22.447
6	64	65	9.846153846	101	1524	11.188
7	128	129	9.922480620	151	3074	8.428
8	256	257	9.961089494	351	6014	9.926
10	1024	1025	9.990243902	1401	24224	9.841
11	2048	2049	9.995119571	2802	48473	9.833
12	4096	4097	9.997559190	5401	97374	9.546

When using MMCM to generate two 10MHz clocks with a phase difference of 10° , the actual output phase difference of MMCM is 9.9° . When N is taken as 3, 4, and 5, the measured phase difference is significantly different from the actual phase difference, and the measurement is not accurate at this time. As the N value increases to 8, the measured phase difference approaches 9.9° . When N is taken as 9, the output

clock signal is partially synchronized and cannot be measured (please provide an explanation). When N is taken as 12, the amplification factor is multiplied, and the counting clock frequency is 500MHz, with a period of 2ns, the measurement accuracy can reach $2 / 4097 \approx 488 fs$.

Table 2. Phase Counting Measurement of 500MHz to 125MHz Signal

N	2^N	$2^N + 1$	f_{offset} (MHz)	pos_cnt	neg_cnt	$\Delta\theta$ ($^\circ$)
4	16	17	117.647058824	4	64	10.590
6	64	65	123.076923077	8	122	11.077
7	128	129	124.031007752	16	246	10.909
8	256	257	124.513618677	31	471	11.116
10	1024	1025	124.878048780	144	1929	12.504
11	2048	2049	124.938994632	348	3882	10.809

When using MMCM to generate two 125MHz clocks with a phase difference of 10° , the actual output phase difference is 11.25° . When N is taken as 11, the amplification factor is $2^{11} + 1 = 2049$ times, and the counting clock frequency is 500MHz, with a period of 2ns, the measurement accuracy can reach $2 / 2049 \approx 976fs$.

4. Conclusion

By comparing and analyzing multiple test results, the following conclusions can be drawn:

(1) Small phase differences can be measured through digital dual mixing, and the measurement accuracy can reach sub-nanosecond level;

(2) Choosing an appropriate auxiliary beat frequency can reduce or eliminate burrs and interference after mixing. When the amplification factor is small, there is an error in the measured phase difference; When the magnification is large, burrs appear on the edges, and the larger the magnification, the wider the width of the burrs. Therefore, it is necessary to choose a reasonable amplification factor.

Acknowledgment

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