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Review of Threshold Voltage Modeling for Nitride Recessed-Gate FinFETs under Thermal Effects

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Abstract: The nitride-based (for instance, GaN) recessed gate FinFET has potential applications in the high frequency and high power sectors owing to its large bandgap properties and excellent channel controllability. Nevertheless, the problem of self-heating caused by the downsizing of the devices results in the drift of threshold voltage. This paper systematically reviews the current research status of threshold voltage modeling for nitride recessed-gate FinFETs under thermal effects. First, key domestic and international achievements in self-heating effect characterization, recessed-gate technology, and threshold voltage modeling are summarized. Second, the regulation rules of structural parameters and heat dissipation schemes on thermally induced threshold voltage drift are generalized, establishing key quantitative relationships: every 10 nm increase in recess depth causes a positive threshold voltage shift of 30–50 mV, and a high-thermal-conductivity substrate can reduce the hot-spot temperature in the channel by 20–30 K. Finally, deficiencies in current research are analyzed, including insufficient revelation of thermoelectric coupling mechanisms, lack of multiphysics modeling, and inadequate quantification of process-induced thermal damage. This paper points out that future efforts should focus on thermoelectric co-modeling and optimization of thermal management structures, providing theoretical support and engineering references for accurate threshold voltage modeling and device structure optimization of nitride recessed-gate FinFETs under thermal effects.

Keywords: Nitride; Recessed-gate FinFET; Threshold Voltage; Self-heating Effect; Thermoelectric Coupling.

1. Introduction

As semiconductor technology advances toward the 3 nm node and beyond, traditional silicon-based devices are approaching physical limits. Nitride-based wide bandgap semiconductors (such as GaN) with high critical electric field (~3.3 MV/cm) and high electron saturation velocity (~2.5 x 10^7 cm/s) have made suitable choices for high frequency and high power applications in the coming generation. In particular, the recessed-gate FinFET technology offers improved gate control by wrapping three-dimensional gates around the channel, which modifies the threshold voltage.

However, the self-heating effect caused by high integration density leads to a significant local temperature rise in the channel, inducing threshold voltage drift and severely threatening device reliability and modeling accuracy. Son et al. first revealed the mechanism by which self-heating exacerbates negative bias temperature instability (NBTI) degradation in nanoscale bulk FinFETs, showing that self-heating-induced local temperature rise can shorten NBTI lifetime by more than an order of magnitude [1] . Furthermore, Mao revealed that the cumulative effect of quantum coupling and self heating on the threshold voltage of GaN MIS HEMTs has not yet been addressed by any model [2]. At present, most of the work is being done for silicon devices, and there is no review available about the mechanisms of thermoelectric coupling in nitrides. There is a research gap regarding the integration of “nitride,” “recessed gate,” and “thermal effect.”

On this account, this paper comprehensively reviews the research results of threshold voltage modeling of nitride recessed gate FinFETs in thermal effect, studies the thermoelectric interaction principle, summarizes the adjustment rule of the structural parameter, and points out the deficiency of the present study.

2. Device Physics Fundamentals of Nitride Recessed-Gate FinFETs

2.1. Nitride Material Properties

Gallium nitride (GaN), which is an example of a III V wide bandgap semiconductor, possesses a band gap of 3.4 eV (Silicon: 1.12 eV). The polarization mechanism in the heterojunction of AlGaN and GaN creates a very high-density two-dimensional electron gas (2DEG) with a mobility of up to 1500-2000 cm2/(Vs). The thermal conductivity of GaN is estimated to be 130 W/(m·K).

2.2. Structural Characteristics of Recessed-Gate FinFETs

Recessed gate FinFET is created by the formation of recessed structure, where the gate will be brought near to the channel region in order to improve gate controllability and minimize the occurrence of short-channel effects. As the recess depth increases, the AlGaN layer thickness decreases. As a consequence, the density of 2DEG decreases and thus there is a positive change in threshold voltage. Additionally, the recessed gate structure helps increase the transconductance and frequency performance. Wang et al. proposed an analytical model for threshold voltage of GaN based recessed gate FinFETs [3].

2.3. Threshold Voltage Extraction Methods and Nitride Specificity

There are three primary techniques available for extracting threshold voltage: the linear extrapolation technique (simplest but susceptible to noise interference), the constant current technique (most intuitive but arbitrary in selecting a reference current level), and the second derivative technique (physically relevant, applicable for precise analysis).

The 2DEG in nitride HEMT devices is dominated by polarization effects, hence the threshold voltage measurement should include polarization charge effect. Also, the nitride devices have high interface trap density and hysteresis effect, hence consideration of sweep direction. Nitride devices operate at higher voltages with higher power density, leading to more significant self-heating effects; moreover, polarization intensity is temperature-sensitive, necessitating an independent theoretical framework for thermal effect modeling.

3. Self-Heating Effect and Threshold Voltage Drift Mechanisms

3.1. Physical Origin of the Self-Heating Effect

The self-heating effect originates from Joule heat generated by the channel current. Electron-phonon scattering transfers energy to the lattice, causing a local temperature rise. In the three-dimensional FinFET structure, the fin is surrounded by insulating dielectrics; heat conduction relies mainly on source/drain contacts and the substrate, and the hot-spot temperature in the channel is significantly higher than the substrate temperature. Do Gyun An et al. performed 3D TCAD simulations to analyze the effect of channel-to-drain spacing on self-heating in 14 nm SOI-FinFETs, finding that reducing this gap lowered the maximum lattice temperature by 29.8 K [4].

3.2. Influence of Temperature on Threshold Voltage

Temperature rise affects threshold voltage through the following mechanisms: bandgap narrowing with temperature (GaN temperature coefficient ∼−0.5 meV/K), increasing intrinsic carrier concentration; shift of the Fermi level, altering surface inversion conditions; enhanced lattice vibrations increasing carrier scattering and reducing mobility; and changes in interface trap charge/discharge states, modifying effective gate control capability. Parihar et al. performed thermal, DC, and RF characterization of 5 nm FinFETs, quantifying the temperature effect on threshold voltage (∼70 mV/165 K) and modifying the BSIM-CMG model using a thermal network equivalent circuit [5].

3.3. Coupling of NBTI and Self-Heating: Differences between Nitride and Silicon

Negative bias temperature instability (NBTI) couples with the self-heating effect. Compared to silicon devices, nitride devices operate at much higher voltages (tens to hundreds of volts) and can experience channel temperature rises of 100–200 K. The GaN/AlGaN heterojunction interface contains a large number of donor-like traps, and NBTI degradation primarily arises from trap charging/discharging. Yan Liu et al. systematically investigated the effects of thermal surface contact resistance, fin width, and temperature on NBTI under self-heating conditions, finding that self-heating significantly accelerates the charging/discharging rate of interface traps, and that NBTI degradation is more severe in narrow-fin devices [6]. Additionally, the high electric field promotes hot-carrier injection, which couples intricately with self-heating, demanding an independent theoretical framework.

4. Current Status of Threshold Voltage Modeling

4.1. International Research Progress

Parihar et al. developed a thermal effect model for 5 nm FinFETs that shows excellent agreement with measured data, but the model parameters rely on extensive experimental data, and stress effects are not considered [5].

Do Gyun An et al. provided quantitative relationships between structural optimization and thermal performance improvement, but did not develop a compact model [4].

The work done by Singh et al. provides an analytical model for determining the threshold voltage in GaN SOI FinFETs through the use of Poisson equation, taking into account the effect of high k-gate dielectric and underlap [7]. This model correlates reasonably with experimental results, but the effect of self heating is not taken into consideration.Wang et al. have suggested a self heating effect modeling scheme in FinFETs that takes into account characteristic parameters and hence has wide application and accurate estimation of channel temperature rise and threshold voltage variation [8].

4.2. Domestic Research Progress (China)

Some representative works related to the threshold voltage of the recessed gate GaN FinFET include the work carried out by Wang et al. of Xidian University [3], where the threshold voltage model of AlGaN/GaN recessed gate FinFETs of various fin sizes was analytically modeled through the effect of recess and fin size. The model has high precision since its deviation is less than 8% from the experiment results. Considering the recess region as stepped AlGaN, the analysis found that each 10-nm recess depth increases the positive shift of threshold voltage of 30–50 mV. No thermoelectric coupling physical mechanism has been proven so far.

In regard to the processing and thermal issues, the domestic research work mainly concentrated on the fabrication process and structure design.

4.3. Comparison of Domestic and International Research

In international research, greater attention is paid to model calibration and simulation with an eye toward generality of models and development of PDK, while the problem of accounting for thermal influences and multiphysics interaction parameters are considered in a more systematic way (for example, [2,6]). In domestic research, greater attention is paid to experimental studies and structural optimization, which has provided a rich experience in fabrication of devices, but still lags behind international research in terms of systematic studies of thermoelectric interaction.

5. Regulation Rules of Structural Parameters and Heat Dissipation Schemes

5.1. Influence of Recess Depth

The threshold voltage becomes positive and changes linearly by about 30–50 mV per 10 nm of increase in the depth of the recess ranging from 0 nm to 50 nm. As recess depth increases, the thickness of the AlGaN layer is decreased and thus 2DEG density is reduced. This can be explained through the model developed by Wang et al. [3].

5.2. Influence of Fin Width

Increasing fin width from 100 nm to 200 nm causes a negative threshold voltage shift of about 0.15 V and an increase in transconductance of about 20%. Narrow fins (<50 nm) improve gate control capability, achieving subthreshold swing below 80 mV/dec, but parasitic resistance increases by about 30%, necessitating a trade-off between gate control efficiency and on-resistance. Yan Liu et al. noted that narrow-fin devices exhibit more severe NBTI degradation under self-heating, adding a new reliability constraint to fin width design [6].

5.3. Gate Dielectric Engineering

High-k dielectrics (HfO_2, Al_2O_3) can reduce gate leakage current while maintaining the equivalent oxide thickness. The Al_2O_3/GaN interface has a relatively high trap density, leading to increased subthreshold swing and reduced channel mobility; improving interface quality is critical. Mao demonstrated that quantum coupling effects interact with self-heating effects in high-k gate dielectric structures, jointly modulating threshold voltage; neglecting quantum coupling in traditional models leads to significant errors [2].

5.4. Optimization of Heat Dissipation Schemes

Regarding substrate engineering, replacing a sapphire substrate with a diamond substrate (thermal conductivity 2000 W/(m·K)) can lower the channel hot-spot temperature by 20–30 K and reduce threshold voltage drift by about 30%. Do Gyun An et al. proved that optimizing contact spacing reduces the maximum lattice temperature by 29.8 K [4]. Although SOI structures reduce parasitic capacitance, the low thermal conductivity of the buried oxide layer exacerbates self-heating; this can be mitigated by embedding high-thermal-conductivity metal layers in the buried oxide to form thermal vias. The self-heating modeling method of Wang et al. can be used to evaluate the temperature-rise suppression effect of different heat dissipation structures [8].

6. Existing Problems and Future Prospects

6.1. Main Shortcomings of Current Research

Insufficient revelation of thermoelectric coupling mechanisms. Most existing studies treat thermal effects as an independent factor, lacking a systematic analysis of thermoelectric coupling. Although Mao revealed the combined influence of quantum coupling and self-heating on threshold voltage, the study is limited to specific device structures and has not been extended to recessed-gate FinFETs [2]. The temperature dependence of nitride polarization intensity is rarely incorporated into models.

Lack of unified multiphysics modeling. There is no unified model simultaneously considering electrical, thermal, and stress effects. Parameters of BSIM CMG after modification have no physical significance and cannot be applied to other structures. Though Yan Liu et al. have associated NBTI with thermal aspects, still a comprehensive analytical approach is yet to be developed [6].

Inadequate quantification of thermal damage arising from process. The impact of processes like etching and annealing on thermal effects is generally explained qualitatively without any quantitative model that takes process variables into consideration.

Limited applicability of the model. Currently available models have been developed for particular ranges of structural parameters (for instance, fin width of 50-200 nm and recess depth of 0-50 nm, [3,7]) and cannot be used for nodes of 3 nm and below.

6.2. Future Research Directions

Thermoelectric co-modeling. TCAD simulations in combination with experimental results should be used to formulate the physics model incorporating the effects of temperature dependent polarization and temperature dependent trapping. The combined study of quantum coupling/self-heating by Mao [2] can be expanded to recessed gate FinFETs.

The machine learning helped with model calibration. Training surrogate models using multiple group process temperature threshold voltage data can help to extract and extrapolate parameters rapidly. Modeling technique by Wang et al. can be used as scalable parameterization technique that is compatible with machine learning [8].

Thermal-process co-optimization. Design orthogonal experiments for acquiring data on threshold voltages at various process conditions, create process performance maps through response surface methodology, and optimize the process window using multi-objective optimization algorithms.

Exploration of novel heat dissipation structures. Design embedded heat dissipation, through-fin heat dissipation, and other structures via TCAD simulations, and evaluate their impact on channel temperature distribution and threshold voltage using modeling methods such as those in Refs. [4,8].

7. Conclusion

Nitride recessed-gate FinFETs hold great promise for high-frequency and high-power applications, but threshold voltage drift caused by the self-heating effect is a core bottleneck. This paper systematically reviews the current status of threshold voltage modeling for nitride recessed-gate FinFETs under thermal effects, summarizes key domestic and international achievements, and generalizes the regulation rules of structural parameters (every 10 nm increase in recess depth causes a positive threshold voltage shift of 30–50 mV; every 50 nm decrease in fin width causes a positive threshold voltage shift of about 0.15 V) and heat dissipation schemes (a diamond substrate can reduce the channel hot-spot temperature by 20–30 K). Deficiencies in the revelation of thermoelectric coupling mechanisms, multiphysics modeling, and quantification of process-induced thermal damage are analyzed. The future work should pay attention to thermoelectric co-modeling, model calibration using machine learning techniques, thermal processing co-optimization, and research on new heat dissipation architecture design, which could provide theoretical foundation and engineering references for precise threshold voltage modeling and device structure optimization under thermal effect for nitride recessed gate FinFETs.

References

[1] Son, D., Hong, K., Shim, H., Pae, S., & Shin, H. (2019). New insight into negative bias temperature instability degradation during self-heating in nanoscale bulk FinFETs. *IEEE Electron Device Letters*, 40(9), 1354–1357. https://doi.org/10._1109/ LED. 2019.2931495.

[2] Mao, L. (2024). Quantum coupling and self-heating impacts on threshold voltages of GaN metal-insulator-semiconductor high-electron-mobility transistors. *Results in Physics*, 160, 107929. https://doi.org/10.1016/j.rinp.2024.107929.

[3] Wang, C., Wang, X., Zheng, X., Wang, Y., He, Y., Tian, Y., et al. (2018). Characteristics and threshold voltage model of GaN-based FinFET with recessed gate. *Chinese Physics B*, 27(9), 098502. https://doi.org/10.1088/1674-1056/aad66c.

[4] An, D. G., Lim, U. H., Song, Y. S., Kim, H., & Kim, J. H. (2025). Analysis of thermal effects according to channel and drain contact metal distance. *Case Studies in Thermal Engineering*, 65, 105642. https://doi.org/10.1016/ j.cset. 2025. 105642.

[5] Parihar, S. S., Pampori, A., Dwivedi, P., Huang, J., Wang, W., Imura, K., et al. (2023). A comprehensive RF characterization and modeling methodology for the 5nm technology node FinFETs. *IEEE Journal of the Electron Devices Society*, 11, 444–455. https://doi.org/10.1109/JEDS.2023.3270992.

[6] Liu, Y., Ma, Y. H., & Pan, C. (2024). An investigation into the thermal surface contact resistance, fin width and temperature on negative bias temperature instability during self-heating. *Microelectronics Reliability*, 157, 115414. https://doi.org/ 10. 1016/ j.microrel.2024.115414.

[7] Singh, S., Dhar, R. S., Ahmad, H., & Hussein, M. I. (2025). Exploration and analysis of high-K wrapped underlap based GaN SOI FinFET for enriched performance towards RF applications. *Materials Today Electronics*, 14, 100170. https://doi.org/10.1016/j.mtel.2025.100170.

[8] Wang, Y., Liang, H., Li, D. Q., Zhang, H., Shao, Z. W., Pan, Y. Q., et al. (2025). A modeling method for self-heating effect of FinFET with wide application range considering characteristic parameter. *Physica Scripta*, 100(3), 035937. https://doi.org/10.1088/1402-4896/ad7b31.