International Journal of Energy
ISSN: 2957-9473 | Vol. 2, No. 3, 2023

Effects of Silicon Wafer's Resistivity on Passivation and Devices Performances of Solar Cell

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Abstract: In the manufacture of solar cells, the resistivity of silicon wafers has a crucial impact on their performance. This study investigated the effects of different resistivities on p-TOPCon solar cells. The results indicate that lower resistivity wafers have a higher implied open-circuit voltage (iV_{oc}) value, but higher carrier mobility due to the low resistivity leads to an increase in saturation current density (J_0). Conversely, solar cells made on higher resistivity silicon wafers have a lower carrier mobility, leading to slower electron-hole recombination and lower bulk recombination, resulting in the advantage of lower saturation current density and higher minority carrier lifetime. At the same time, simulation shows that as the resistivity increases, the V_{oc} and efficiency increase. However, cost considerations need to be taken into account as higher resistivity silicon wafers are more expensive. Therefore, resistivity between 2 - 3 $\Omega \cdot cm^2$ is considered the preferred substrate for solar cells as it offers a better balance between cost and achieving high cell efficiency.

Keywords: TOPCon; Passivation; Resistivity.

1. Introduction

Photovoltaic power generation has become one of the most cost-effective sources of renewable energy, and is expected to reach global grid parity within the next 3-5 years as its price continues to decrease. With its decreasing cost, photovoltaic power generation is poised to become one of the primary and most cost-effective sources of renewable energy, as well as a key driver of China's energy structure transformation.

Tunnel oxide passivated contact (TOPCon) solar cells technology has started to enter industrialization and is becoming a mainstream technology due to its advantages over other technologies.[1–3] With only a few core equipment additions, it can easily upgrade and replace passivated emitter and rear contact (PERC) production lines. The core structure of TOPCon technology includes ultra-thin oxide silicon and heavily doped poly-Si silicon film, which play important roles in passivation. The oxide silicon passivates dangling bonds on the surface of silicon wafers, inhibits minority carriers from entering the poly-Si silicon layer, and captures hydrogen atoms.[4,5] Meanwhile, heavily doped poly-Si and surface diffusion doping atoms reduce the concentration of minority carriers in the surface area.[6–8]Overall, TOPCon technology has great potential to further reduce the cost of photovoltaic power generation.

Solar cell efficiency and performance are influenced by numerous factors, and the resistivity of silicon wafers is a critical one[9]. During the manufacturing process, silicon wafers need to be doped with specific elements, usually boron or phosphorus, to achieve desired electrical properties. Generally, higher doping concentration results in lower resistivity of silicon wafers. The resistivity of silicon wafers affects the current flow and loss in solar cells, thus directly impacting their conversion efficiency.

Optimizing the resistivity of silicon wafers is, therefore, a crucial strategy to enhance solar cell efficiency. However, currently, the specific impact of silicon wafer resistivity remains unclear. This paper delves deeper into this subject and reveals that a low resistivity yields a high implied open-circuit voltage (iV_{oc}), yet it also leads to an increase in saturation current density (J_0) and a decrease in minority carrier lifetime (τ). On the other hand, higher resistivity in silicon wafers reduces carrier mobility, leading to slower electron-hole recombination, lower bulk recombination, and a lower saturation current density, resulting in higher minority carrier lifetime. In solar cells, as the resistivity of the silicon wafer increases, V_{oc} and efficiency both gradually increase.

However, the purity of silicon wafers increases with higher resistivity, leading to higher production costs. Therefore, a balance must be achieved between wafer resistivity and passivation to increase solar cell efficiency while maintaining cost advantages.

2. Experiments

Passivation samples were prepared using planar p-type CZ c-Si wafers, which had a thickness of 165 μm and a resistivity (R) of 0.8 - 6 Ω·cm. The wafers were first polished with an alkaline solution, followed by standard RCA cleaning. High concentration ozone gas (400 mg/L) was then generated and flowed into the diffusion furnace. After removing the as-grown oxide layer by immersing the wafers in 5 vol.% HF solution, they were subjected to oxidation at 400°C for 10 min. A 30 nm layer of boron-doped amorphous silicon was subsequently deposited on both sides of the ultra-thin SiO_x coated wafers using an RF PECVD system. The crystallization of amorphous Si and activation of B dopant were performed by high temperature annealing at 800-1000°C for 30 minutes with N_2 atmosphere, followed by wet N_2 hydrogenation and aluminum oxide hydrogenation. The photo-conductance decay (PCD) can be measured by Sinton WCT-120 from which τ_{eff}, iV_{oc} and J_0 for passivation quality characterization can be attained. The simulation was carried out using the free-version Quokka 2.5.

3. Results and Discussion

The iV_{oc} is a critical parameter that serves as a key indicator of the efficiency and passivation quality of solar cells. The resistivity of silicon wafers plays a significant role in determining iV_{oc}, as shown in Figure 1. Except for annealing at 840°C, passivation samples made from low-resistivity silicon wafers (LW) exhibit considerably higher iV_{oc} than those made from high-resistivity silicon wafers (HW), with a maximal increase of 5 mV. Notably, we also observed that HW samples exhibit a higher iV_{oc} under low-temperature annealing, suggesting their superiority under such conditions.

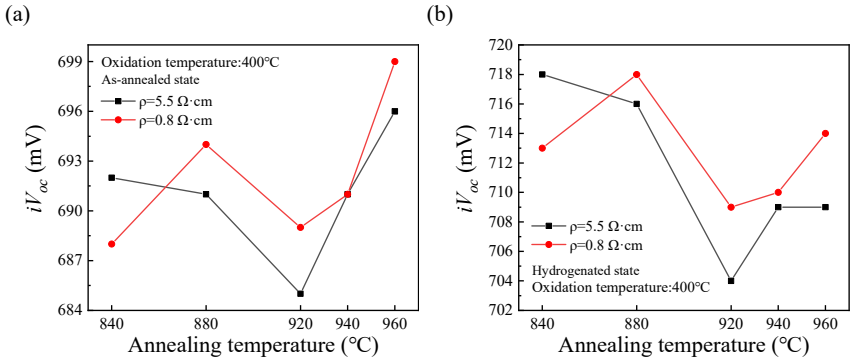

Figure 1. (a-b) iV_{oc} of the as-annealed and AlO_x hydrogenated p-TOPCon lifetime samples.

J_0 is a crucial indicator of passivation, and its value is also a key parameter to consider. As shown in Figure 2, it is evident that the J_0 value for LW is higher than that for HW, indicating a negative impact of LW. This can be attributed to the fact that when the resistivity of the silicon wafer is high, electrons move more slowly in the silicon, and charges take longer to reach the electrode, thereby limiting the flow of current. Therefore, HW will generate greater resistance to charge transport, resulting in a decrease in saturation current density. Conversely, when the resistivity of the silicon wafer is low, electrons move faster in the silicon and charges reach the electrode more quickly, resulting in faster current flow. As a result, LW generates less resistance to charge transport, leading to an increase in saturation current density.

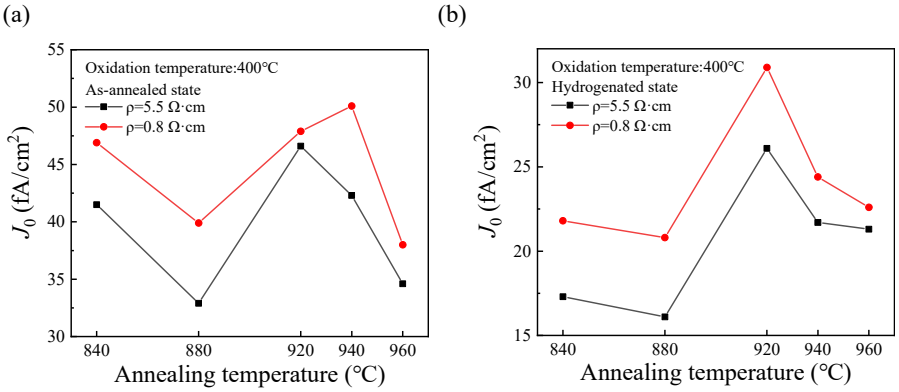

Figure 2. (a-b) J_0 of the as-annealed and AlO_x hydrogenated p-TOPCon lifetime samples

Similarly, the resistivity of a silicon wafer has a significant impact on minority carrier lifetime. As resistivity increases, the mobility of charge carriers decreases, causing a reduction in the rate of electron-hole recombination in solar cells. This leads to a decrease in bulk recombination and an increase in minority carrier lifetime. As shown in Figure 3(a, b), the τ of HW is much higher than that of LW, with a maximum difference of 2000 μs. Additionally, Figure 3(c) reveals that low silicon wafer resistivity helps to reduce $J_{0,bulk}$ from 30.6 to 19.5 fA/cm^2 (Δn = 1×10^{15} cm^{-3}). The corresponding contacts, shown in Figure 3(d), satisfy the requirements for solar cell fabrication.

Equation (1) is the formula for calculating resistivity. It can be seen that resistivity is affected by both carrier concentration and mobility. At low resistivity, the doping concentration is higher and recombination is more likely to occur.

$$\rho = \frac{1}{pq\mu_p} \quad (1)$$

ρ is silicon wafer resistivity, p is carrier concentration in p-type silicon wafers, q is the charge, and μ_p is the mobility of charge carriers in p-type silicon wafers.

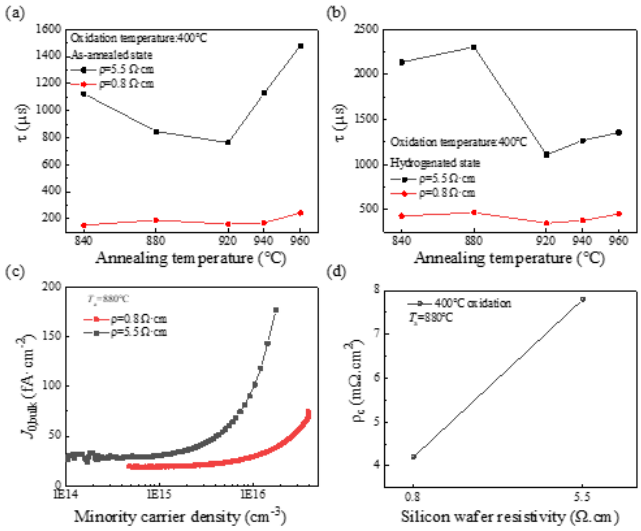

Figure 3. (a-b) τ of the as-annealed and AlO_x hydrogenated p-TOPCon lifetime samples. (c) The $J_{0,bulk}$ after hydrogenated, annealed at T_a=880°C. (d) Contact resistivity measured by TLM method, annealed at Ta = 880°C.

Table 1. N_A and $\tau_{intrinsic}$ of different wafer resistivity

Wafer Resistivity (Ω·cm)	N_A (cm^{-3})	$\tau_{intrinsic}$ (μs)
0.8	1.93612E+16	448.6
5.5	2.50372E+15	3924.7

Finally, we simulated the performance of p-TOPCon solar cells using Quokka 2.5 and predicted the results for HW and LW. The simulation results are presented in Figure 4, with the corresponding parameters listed in Table 2. Furthermore, Table 1 illustrates the relationship between silicon wafer resistivity and lifetime. By solely altering the resistivity of the silicon wafer, it can be observed that V_{oc} increases with the increase of the resistivity of the silicon wafer, which is inconsistent with the trend of iV_{oc}. The reason for this inconsistency is that the recombination loss of metal and silicon is not considered under the sinton test. It can be noticed that increasing wafer resistivity helps to reduce the intrinsic and SRH recombination losses, as shown in Figure 4 (c).

Table 2. Parameter for simulations

structure	TOPCon
Cell thickness	165 μm
p-type bulk resistivity	Variable
Bulk lifetime	Variable
Auger model	Richter 2012
Generation current	43.12
Series resistance	0.1 mΩ·cm^2
Shunt resistance	1×10^5 Ω·cm^2
Front Side:	
Front contact shape	Line, width 20μm
Finger space	600 μm
Junction depth, n^{++}	500 nm
Front $J_{0,met}$	20 fA/cm^2
Front $R_{sheet,\ n++}$	90 Ω/sq
Front width of n^{++}	20 μm
Front $J_{0,\ n++}$	20 fA/cm^2
Junction depth, n^+	200 nm
Front $J_{0,pass}$	20 fA/cm^2
Front $R_{sheet,\ n+}$	140 Ω/sq
Front contact resistivity	0.1 mΩ·cm^2
Rear Side:	
Rear contact shape	Full
Finger space	600 μm
Junction depth, p^+	300 nm
Rear $R_{sheet,\ p+}$	30 Ω/sq
Rear J_0 Rear $J_{0,met}$ Rear contact resistivity Optical model: Passivation & Reflectance Layer (SiN_x, n=2) Shading width of finger Z_0	5 fA/cm^2 10 fA/cm^2 1 mΩ·cm^2 SiO_2 2 nm SiN_x 73 nm 100% 6

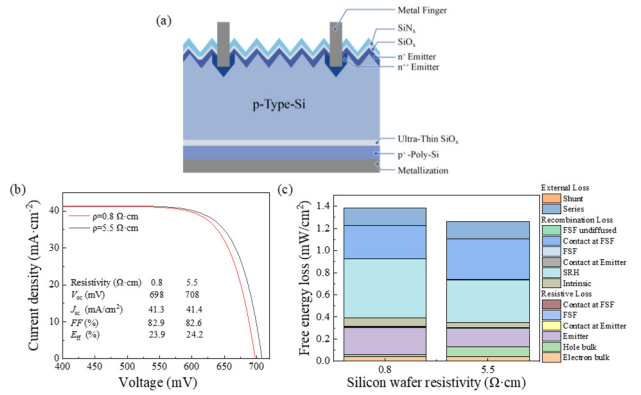

Figure 4. (a) The simulated light *I–V* curves of resistivity of different silicon wafers. (b) The simulated light I–V curves and (c) the free energy loss analysis (FELA) of different silicon wafers resistivity

4. Conclusion

Silicon wafers are the foundation for manufacturing solar cells. This study investigates the impact of different resistivities of silicon wafers on the passivation and efficiency of p-type TOPCon solar cells. The result reveals that low-resistivity wafers have the advantage of a high iV_{oc}, but also exhibit an increase in saturation current density due to faster carrier mobility. As the resistivity of the silicon wafer increases, carrier mobility decreases, leading to slower recombination rates and a decrease in saturation current density. This makes high-resistivity wafers favorable due to their low saturation current density and high carrier lifetime. At the same time, it is shown by simulation that as the resistivity increases, the V_{oc} increases and the efficiency increases. It should be noted that higher resistivity wafers are more expensive. Ultimately, a resistivity range of 2 - 3 $\Omega \cdot cm^2$ is recommended as the optimal substrate for solar cells.

Acknowledgments

This work was supported by the Key Research and Development Program of Zhejiang Province (2021C01006).

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